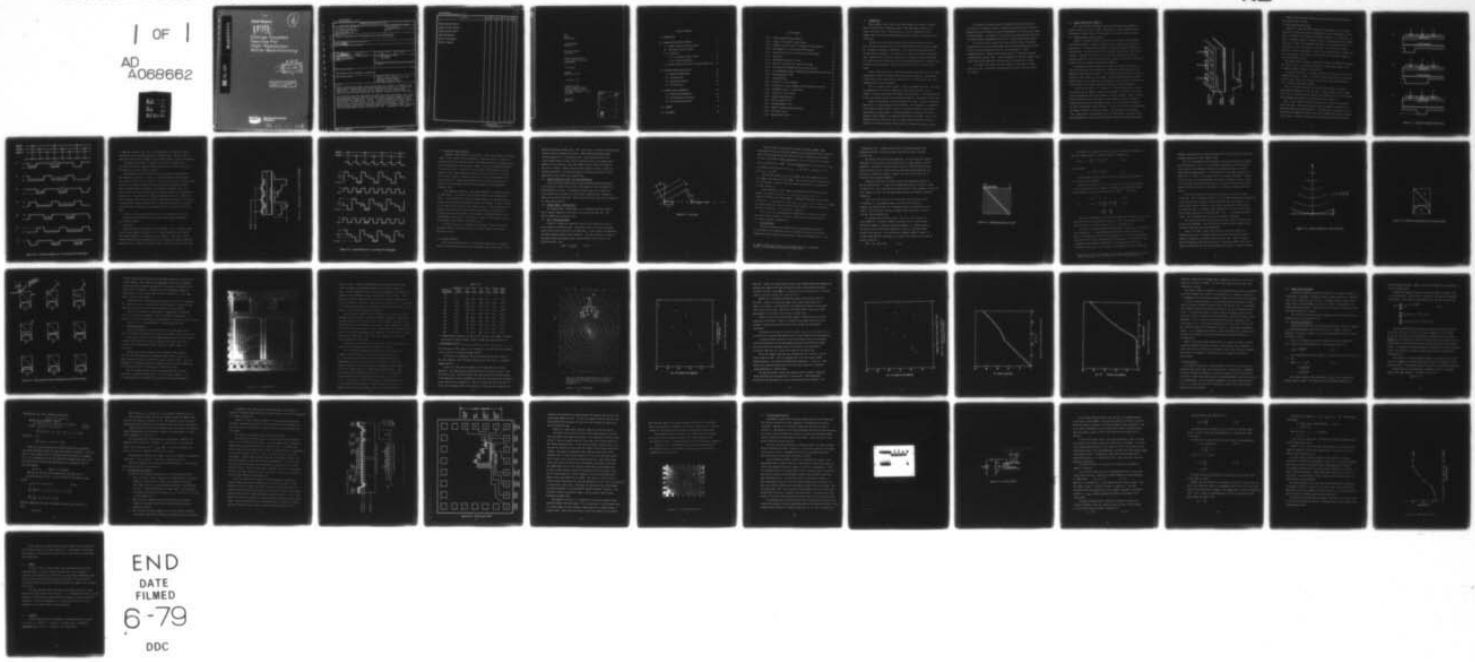
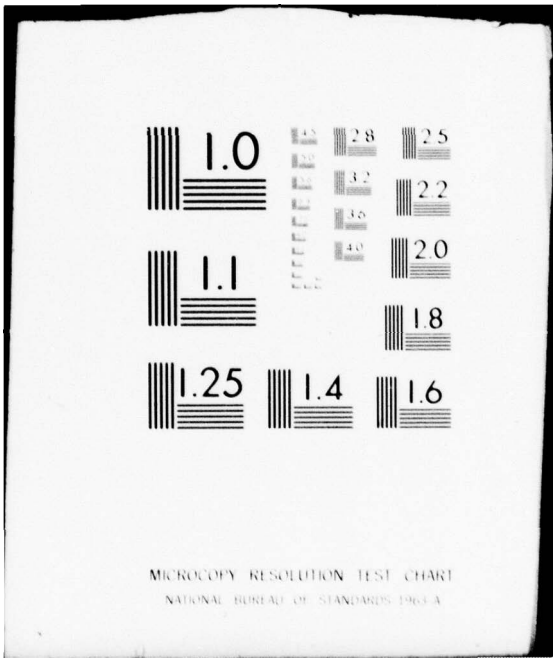
AD-A068 662 BENDIX CORP NORTH HOLLYWOOD CALIF ELECTRODYNAMICS DIV F/G 9/5
CHARGE COUPLED DEVICES FOR HIGH-RESOLUTION SONAR BEAMFORMING.(U)
DEC 78 N00014-75-C-0755

UNCLASSIFIED MC-78-25 NL

1 OF 1
AD A068662



END
DATE FILMED
6-79
DDC


1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963-A

Final Report

LEVEL II

Charge Coupled Devices For High-Resolution Sonar Beamforming

Bendix Electrodynamics Division

Unclassified

Security Classification

DOCUMENT CONTROL DATA - R & D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY (Corporate author)

The Bendix Corporation
Electrodynamics Division
North Hollywood, CA

2a. REPORT SECURITY CLASSIFICATION

Unclassified

2b. GROUP

3. REPORT TITLE

(6) Charge Coupled devices for High-Resolution Sonar Beamforming.

4. DESCRIPTIVE NOTES (Type of report and inclusive dates)

(9) Final Report.

5. AUTHOR(S) (First name, middle initial, last name)

6. REPORT DATE	7a. TOTAL NO. OF PAGES	7b. NO. OF REFS
(11) 4 December 1978 (12) 55p.	49	1

8a. CONTRACT OR GRANT NO.	9a. ORIGINATOR'S REPORT NUMBER(S)
(15) N00014-75-C-0755 new	(14) MC-78-25
8b. PROJECT NO.	
c.	9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report)
d.	

10. DISTRIBUTION STATEMENT

Distribution of this document is unlimited.

11. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY
	Office of Naval Research, Code 222 800 North Quincy Street Arlington, Virginia 22217

13. ABSTRACT

Charge coupled devices (CCD's) were studied under this project to investigate the feasibility of integrating several sonar beamforming functions on a single solid-state "chip". These devices will be very important for multi-element high resolution sonar systems because they are compact, reliable, and use little power.

Two CCD devices have been fabricated and tested with promising results. One is the Charge Coupled Processor (CCP) which performs several functions needed for narrow-band "holographic" beamforming. A four-input CCP experimental device has tested successfully. The other device, the Cascade Charge Coupled Device (C3D), combines several functions required for a broadband time-delay beamformer. A 20-input device has been tested and has performed beamforming for simulated inputs. Descriptions and experimental results of both devices are discussed in this report.

DD FORM 1 NOV 65 1473

UNCLASSIFIED 402 172

Security Classification

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Charge Coupled Devices						
Charge Transfer Devices						
High Resolution Sonar						
Sonar Beamforming						
Acoustic Holography						
Acoustic Imaging						

The
Bendix
Corporation

Electrodynamics
Division

North Hollywood,
California

Charge Coupled Devices for High-Resolution Sonar Beamforming

Final Report

Contract
N00014-75-C-0755

4 December 1978

Sponsored by the
Office of Naval Research
800 North Quincy Street
Arlington, Virginia 22217
Code 222

Report No.
MC-78-25

TABLE OF CONTENTS

LIST OF FIGURES

1.0 INTRODUCTION.

Charge coupled devices (CCD's) were studied under this project to investigate the feasibility of integrating several sonar beamforming functions on a single solid-state 'chip'. These devices will be very important for multi-element high resolution sonar systems because they are compact, reliable, and use little power.

Two CCD devices have been fabricated and tested with promising results. One is the Charge Coupled Processor (CCP) which performs several functions needed for narrowband 'holographic' beamforming. A four-input CCP experimental device has been tested successfully. The other device, the Cascade Charge Coupled Device (C3D), combines several functions required for a broadband time-delay beamformer. A 20-input device has been tested and has performed beamforming for simulated inputs. Descriptions and experimental results of both devices will be discussed in this report.

Charge coupled devices are currently being used in many applications including image sensing, digital and analog signal processing, and memories. Much research is being done on their applications, characteristics, and fabrication, and a wide technology base is being developed.

CCD's are similar in many respects to other semiconductor devices. They share the advantages of reliability, compatibility with other electronic circuit elements, low power and voltage requirements, and compactness. Their manufacturing process uses methods and facilities already developed for semiconductor fabrication.

Charge coupled devices are basically analog in nature. Their most important application is in the manipulation of information. The information is represented by the amount of mobile electric charges in a discrete 'packet' stored within a semiconductor storage element. Such charge packets are transferred to similar adjacent storage elements by the external manipulation of voltages. Due to their inherent structural simplicity, CCD's can perform many information processing functions in a small area while requiring only a few simple controlling signals.

The potential to perform several information processing functions on a single chip is important because it represents a possible practical means of manipulating array information to perform beamforming for high-resolution sonars with many elements. The object of this study was to investigate the feasibility of combining several beamforming functions in a single charge coupled device.

The results of this study of two charge transfer devices, the Charge Coupled Processor and the Cascade Charge Coupled Device, demonstrate the feasibility of custom designed CCD chips for sonar applications. Bendix recommends that this charge transfer device project be continued to develop increased device dynamic range. Further improvement in the CCD's dynamic range could significantly expand the CCD's application to future sonar systems.

This report will discuss the basic concepts of CCDs used in a high-resolution sonar. Descriptions and experimental results of the CCP and C3D will follow.

2.0 CHARGE COUPLED DEVICE CONCEPTS

CCD's are basically semiconductor devices which manipulate information stored as packets of electric charge. The transfer of charge packets from one semiconductor storage element to an adjacent one is known as charge coupling.

2.1 Charge Storage in Potential Wells

Figure 2.1-1 shows a section of a CCD device with three storage elements. A CCD storage element is actually a potential well created at the surface of a semiconductor in a metal-oxide-semiconductor sandwich by applying a voltage to the metal gate. The devices used in this study were made with an n-type silicon substrate. Therefore this section will discuss this particular type of CCD, although p-type CCD's can also be constructed. N-type signifies that the majority charge carriers are electrons and therefore negative.

By applying a negative voltage to the gate, the negative charges will be repelled and the area of the semiconductor immediately under the gate will be depleted of these majority carriers. This creates a potential well where positive charges (or their absence) can be stored. The metal-oxide-semiconductor (MOS) sandwich thus acts as a capacitor and the amount of stored charge is proportional to the product of the charge injection voltage times the MOS capacitance.

The device in Figure 2.1-1 is known as a 'surface' channel device because the minority carriers (that is, the positive charges) are stored at the surface of the semiconductor near the semiconductor-insulator boundary. There is another kind of CCD which has an extra layer of a semiconductor material of opposite conductivity to the other semiconductor layer. This extra layer lies between the other semiconductor and the insulator. In this kind of CCD, the charge packets are stored in the bulk of this extra layer. Thus these devices are known as 'bulk' channel CCD's. Bulk channel devices are more complex in fabrication and more experimental at this time, but they offer potential operational advantages.

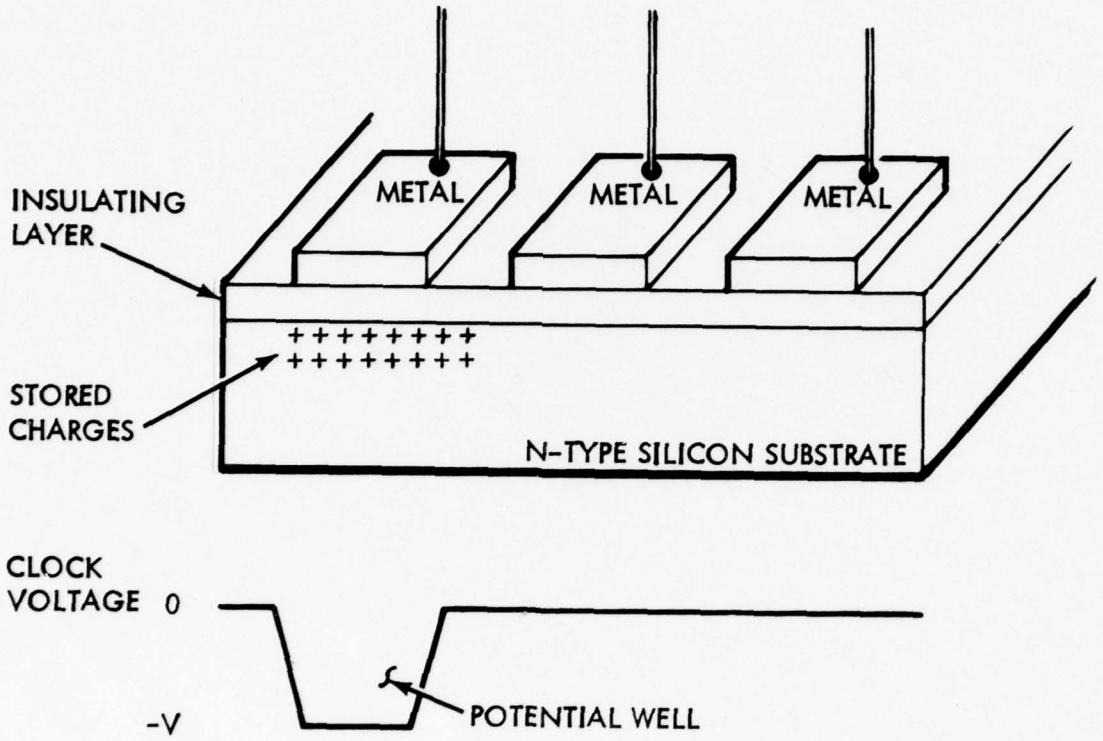


Figure 2.1-1. Charge-Coupled Storage Elements

Both the charge coupled processor and the Cascade Charge Coupled Device are surface channel devices.

2.2 The Charge Transfer Process

Figure 2.2-1 shows the charge transfer process within a CCD. In step 1, the positive charges representing information are stored underneath the first gate in a potential well created by applying a voltage of -V to the gate. In step 2, a negative voltage is applied to Gate 2, allowing the positive charges (or holes) to spread out underneath both gates. As the voltage on Gate 1 is raised back to zero, the charges are attracted to the new area of lowest potential under the second gate. By step 3, the voltage on Gate 1 reaches zero and all the charges in the packet are now under the second gate, completing the charge transfer process.

The charge packet can then be transferred to Gate 3 by repeating the process with Gates 2 and 3. In this way, charge can be shifted down a whole series of storage elements forming a shift register.

In long shift registers, it becomes inconvenient to separately control the voltage on each gate. Figure 2.2-2 shows how every third gate can be connected to one of three clock lines and used to control the charge coupling process. This is known as three-phase clocking.

Step 1 in Figure 2.2-2 shows two discrete packets stored in two wells whose gates are connected to the same clock. When the Phase 2 clock voltages are set to -V, both packets begin moving to the right and by step 3 both packets have completed the transfer to the adjacent well (or 'bucket').

Note in step 2 how the third gate from the left is kept at zero voltage during this step. This forms a potential barrier between the two packets of charge and keeps them from interacting. Thus three gates are needed to contain each unit of information and three clocks with different phases must be used to control them. A group of three gates in this three-phase CCD shift register

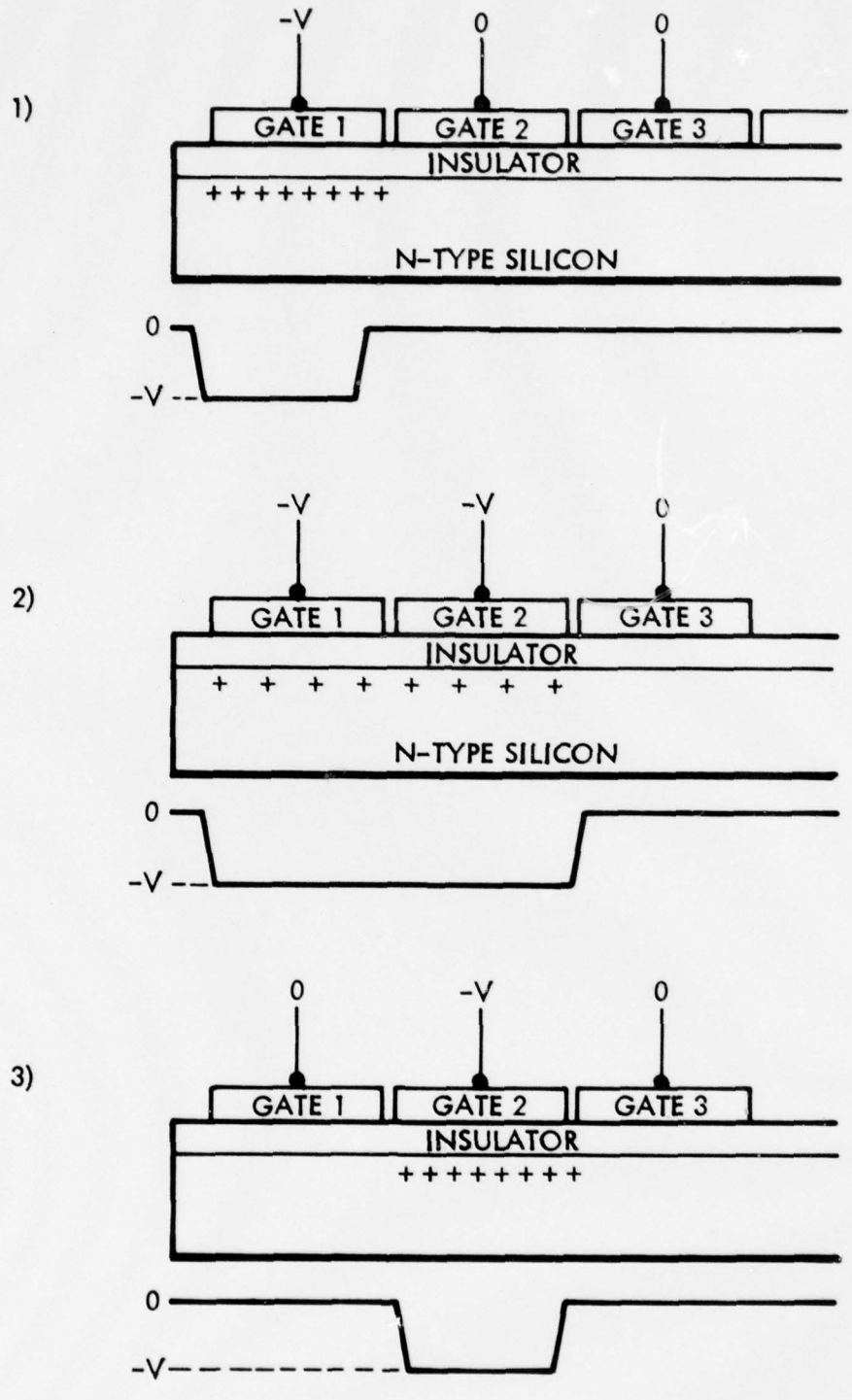


Figure 2.2-1. Stages of the Charge Transfer Process

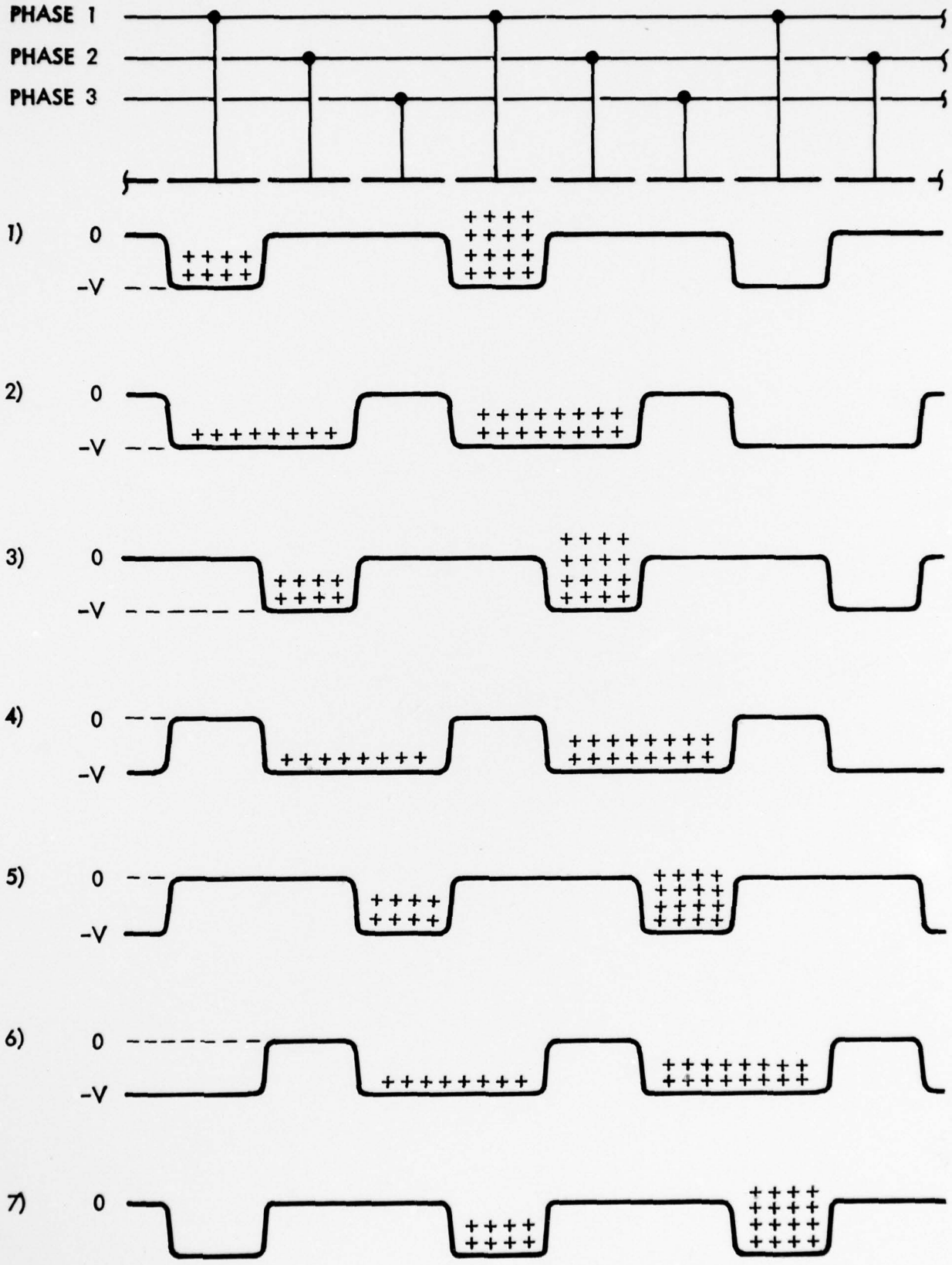


Figure 2.2-2. A Complete Transfer Cycle In a Three-Phase CCD Shift Register

is sometimes referred to as a 'bit' since three gates are required to control and maintain a discrete charge packet or information unit. (The term 'bit' is used rather loosely here to denote a unit of either analog or digital information.)

A minimum of three gates is required to form one bit although four or more gates can be used. However, the more gates per bit, the more clock lines are required to control the shift register.

The minimum of three controlling clocks can be reduced by changing the gate geometry in the device. Figure 2.2-3 shows one means by which the gates in a two-phase device can be constructed. Each gate has two levels of metallization which are at a different distance from the semiconductor-insulator interface where the mobile charges are stored. This provides a potential 'step' of ΔV within a gate since the different insulator thicknesses will affect the potential energy levels. Since both of the gates have two energy levels, it can be seen that a two-phase shift register is actually simulating a four-phase shift register. In this way the different potential levels create potential barriers to prevent the charge packets from moving in the wrong direction or interacting with each other.

Figure 2.2-4 shows a one-bit shift cycle for a two-phase shift register.

Both the Charge Coupled Processor and the Cascade Charge Coupled Device use two-phase shifting.

2.3 Limitations

There are two main limitations on CCD performance. One is incomplete charge transfer which degrades the signal as it is clocked through the shift register. This problem increases as a function of clock frequency. The other is thermal relaxation which causes the potential wells to be filled with thermally generated minority carriers, limiting the length of time a signal can be stored on the chip.

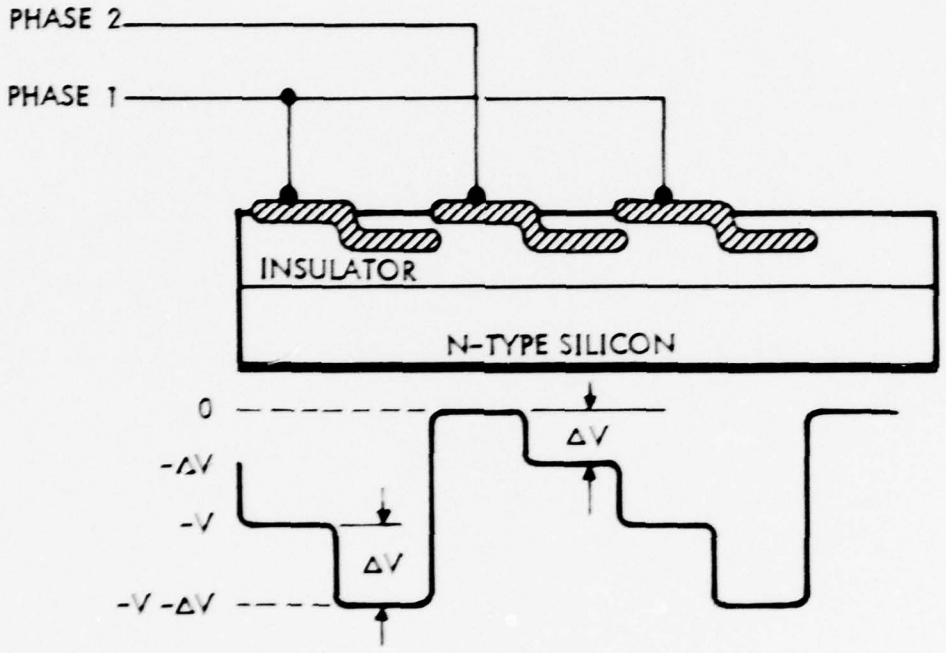


Figure 2.2-3. Gate Geometry in a Two-Phase CCD Shift Register

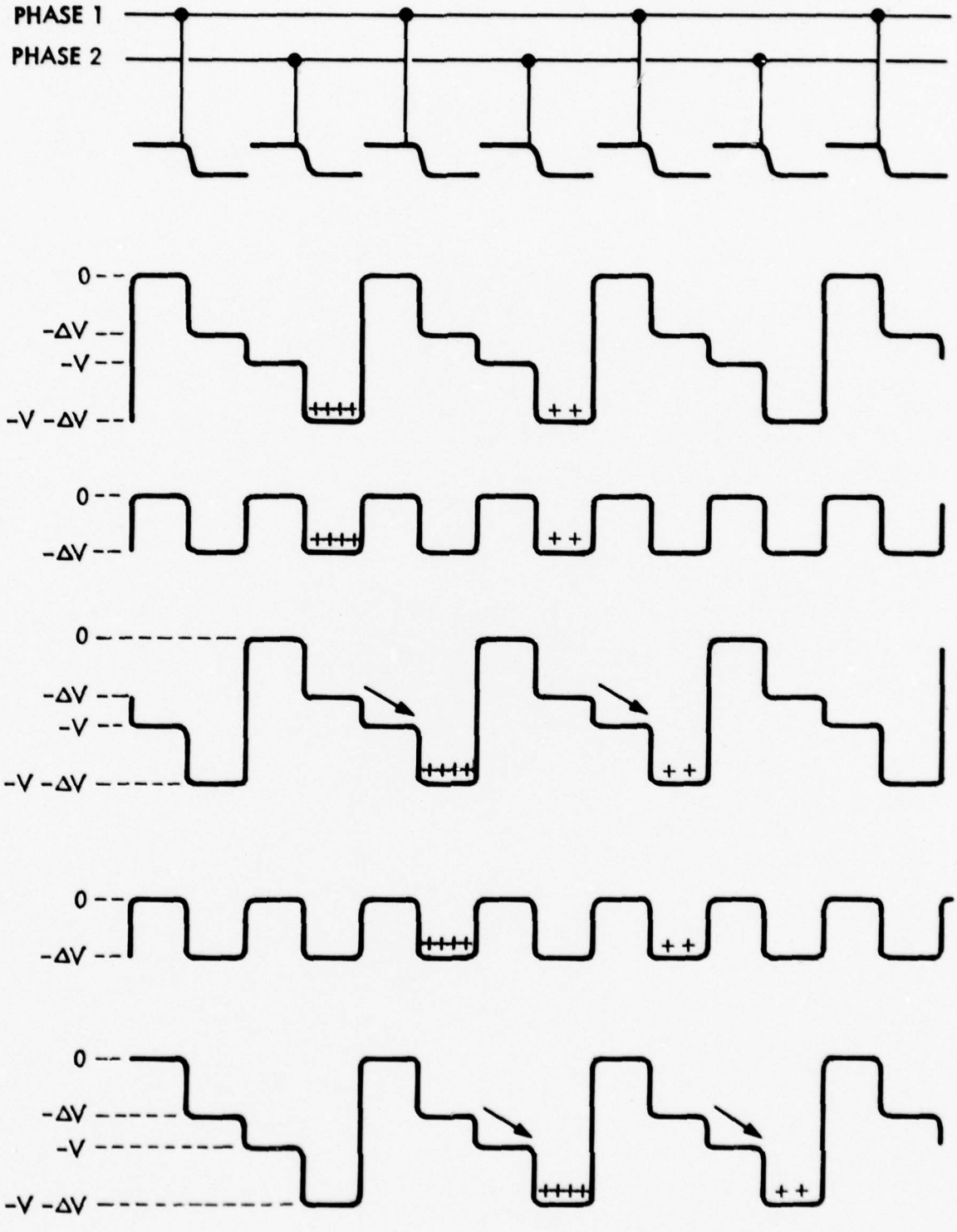


Figure 2.2-4. One-Bit Shift Cycle in a Two-Phase CCD Shift Register

2.3.1 Incomplete Charge Transfer

Incomplete charge transfer has two causes. One is the existence of 'surface states' at the surface of the semiconductor. When the crystal is sliced, the covalent bonds at the edge are severed. These dangling bonds trap charges and re-emit them sporadically causing noise. Surface states are a problem particularly at low signal levels. Their effect can be reduced significantly by using appropriate clock-voltage waveforms and by the use of 'fat zeros', i.e. at zero signal levels a number of minority carriers are stored in the potential well. The second cause of charge transfer inefficiency is high clock frequencies which do not allow enough time for all the electrons to follow the moving potential well.

Three mechanisms combine to induce charge movement to an adjacent region of lower energy: self-induced drift, thermal diffusion, and fringing field forces. Self-induced drift is caused by mutual repulsion of the same polarity charges which spread once the potential barriers are removed. Thermal diffusion arises from the thermal energy of the charge carriers. Self-induced drift and thermal diffusion are the two most important mechanisms of charge transfer. By proper design and application of bias voltages on neighboring gates, field-aided movement can take place. This effect is usually only designed into very high frequency (over 10 MHz) bulk channel devices.

The width of the gate is important in each kind of transfer, therefore designers attempt to keep them as narrow as possible without affecting the fabrication process.

2.3.2 Thermal Relaxation

Just after the depletion well is formed by the application of a negative voltage to the metallization, the silicon conduction band at the surface is well

below the equilibrium energy level. This region attracts randomly drifting minority carriers or holes from the bulk silicon. These thermally generated random carriers eventually fill the potential well. They continually add to the signal charge stored in a well, and will continue to add to the signal packet whenever it is on the chip. Thus, the length of time a signal can remain on the chip is limited. Thermal relaxation time constants of about 1 second are presently obtainable. For many applications, including high resolution sonar beam forming, their effects are insignificant.

2.4 Useful Properties of CCD's for Sonar Beamforming.

CCD's have natural applications to sonar beamforming because many gates can be placed on a single chip and thus large amounts of array information can be manipulated on the chip. By appropriate design, CCD's can be made with time variable shift registers (for delay lines), sampling gates, integration gates, and on-chip multiplexing. The CCP and C3D each use some of these properties of charge coupled devices.

3.0 CASCADE CHARGE - COUPLED DEVICE.

The Cascade Charge - Coupled Device is a time-delay beamformer, meaning that it applies appropriate time delays to array data and then sums. This type of beamforming is discussed next.

3.1 Time - Delay Beamforming.

Figure 3.1-1 shows how a wavefront from an off-axis angle θ arrives at array elements at different times. The parallel lines in the figure represent sound pressure maxima separated by one wavelength. In this figure, the wavefronts are shown reaching element 0 before element n. The time difference is given by the extra distance the wavefront must travel divided by the velocity of the travelling sound. Thus:

$$\Delta t_n(\theta) = \frac{nd \sin \theta}{v} \qquad (3.1\text{-}1)$$

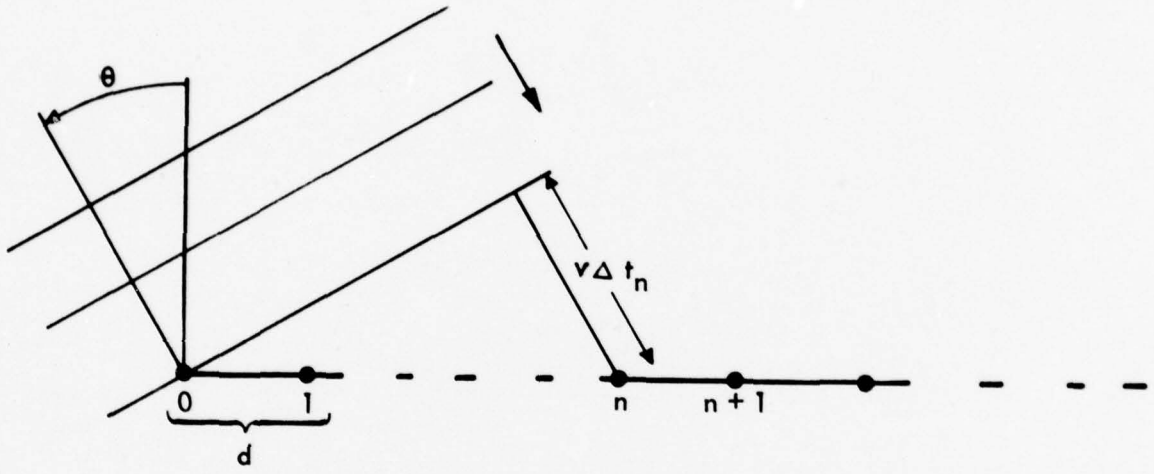


Figure 3.1-1. Time Delay

To form a beam in direction θ, the signals from each element n must be delayed in such a way that they compensate for the different times of arrival. Thus, in an N-element array, the signal arriving at element 0 must be delayed at least a time equal to $\frac{(N-1)\ d \sin \theta}{v}$ which is the time required for the wavefront to reach the last element. The time $\frac{(N-1)d \sin \theta}{v}$ will be referred to as Δt_{max}. For element #1 the delay will be $(\Delta t_{max} - \Delta t\ (\theta))$ and for element n it will be $(\Delta t_{max} - \Delta t_n\ (\theta))$.

Once the time delays from all the elements have been compensated for in this manner, the signals are then summed. This forms one beam in the direction θ. To form beams in another direction requires application of a different set of delay factors Δt_n.

Sonar beamforming is most commonly implemented using this delay-and-sum method. One method of doing this is with tapped LC delay lines. In a system of N elements the maximum number of independent beams that can be formed is equal to N. To beamform with tapped delay lines, each of the N elements is followed by a delay with N taps. When the array has many elements, the size, complexity and power consumption of N^2 taps becomes overwhelming.

The Cascade Charge Coupled Device was developed to simplify the hardware by using the basic properties of CCD's to combine the delay and sum functions on a small, reliable, low-power chip.

3.2 C3D Description.

The basic Cascade Charge Coupled Device was developed by Roger Melen and John Shott of the Integrated Circuits Laboratory at Stanford University*. Although this device performs the functions of time delay beamforming, it is not

*R. Melen subcontracted to Bendix on the CCP and C3D device development specific to sonar applications under this ONR Project.

a tapped delay line. Instead, the C3D uses the difference between clock frequencies applied to various sections of the chip to control variation of delay time.

The C3D uses CCD shift register properties. By controlling the clocking frequency of a shift register, the passage time of a signal through it can be controlled. One means of using CCD shift registers to perform the time delay function would be to put a single shift register behind each element and clock each one at a different frequency. However, this would not be practical in a system containing many hydrophones.

Instead, the C3D uses a two-section delay line behind each element to get the required delay. A sketch of the beamforming section of the C3D is shown in Figure 3.2-1. The present device has twenty parallel shift registers each with the same number of shifts. The two wedge-shaped sections are clocked at different frequencies.

Within each shift register, the charge packet in the section clocked at frequency f_a is transferred directly into the section clocked at frequency f_b without the need for intermediate output and reinsertion of the signals. The two sections are thus 'cascaded' which is why this is called a 'Cascade' Charge Coupled Device.

To see how this gives delay control, consider a signal coming from array element #0. The entire length of the delay line (or shift register) behind this element is clocked at the same frequency, f_a. Charge remains on one shift (or bit) of the shift register for a time $t_a = \frac{1}{f_a}$ before being shifted to the next bit. For an M-bit shift register (actually M equal 47.5 in the current C3D) the time delay ΔT_a is equal to the number of bits times the period in each bit.

Thus: $\Delta T_a = MT_a = M/f_a$ (3.2-1)

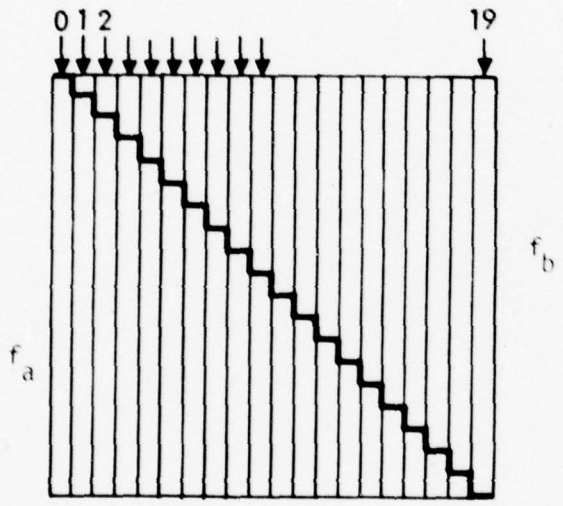


Figure 3.2-1. Beamforming Section of the C3D

For element #1, the first division of 2½ bits is clocked at frequency f_b while the remaining M-2.5(1) bits are clocked at frequency f_a.*

Thus: $$\Delta T_1 = \frac{2.5(1)}{f_b} + \frac{M - 1\ (2.5)}{f_a} \qquad (3.2\text{-}2)$$

and in general:

$$\Delta T_n = \frac{2.5n}{f_b} + \frac{M - 2.5n}{f_a} \qquad (3.2\text{-}3)$$

The time delay from each element thus varies according to the number of bits clocked at each frequency.

Going back to Figure 3.1-1, if it is desired to form a beam in direction θ for an array with spacing d between the elements, the required time delay between elements 0 and 1 must be equal to $\Delta t_1 = \frac{d \sin \theta}{v}$. In the C3D:

$$\Delta t_1\ (\theta) = \Delta T_o - \Delta T_1 \qquad (3.2\text{-}4)$$

or:
$$\Delta t_1\ (\theta) = \frac{M}{f_a} - \left(\frac{2.5}{f_b} + \frac{M-2.5}{f_a} \right) \qquad (3.2\text{-}5)$$

$$= 2.5 \left(\frac{1}{f_a} - \frac{1}{f_b} \right)$$

Any set of two frequencies f_a and f_b which meet this relationship can be used. (Actually there are some practical restraints on their selection which will be discussed later.) To form a beam on-axis, f_a is set equal to f_b.

Thus the C3D can form a beam in one direction by simply using two controlling clock frequencies! To change beamsteering directions, all that needs to be done is to change one or both of these frequencies. One chip can sweep through an entire field of view by changing these two frequencies. Or a parallel system to beamform in M directions simultaneously can be built with M chips each controlled by two clocks. As M increases, the complexity of the C3D processing

* Since one bit consists of two gates in a two-phase shift register, a 'half-bit' refers to one gate. Thus a division with 2-½ bits contains five gates.

hardware increases only by a factor M instead of M^2. This can lead to significant hardware reductions for multi-element arrays.

Not only can beamsteering be performed by the C3D, but near-field focussing can be achieved too. This is a very important consideration in high resolution sonar because as the frequency increases, the minimum range that can use the plane wavefront approximation (i.e. the minimum far-field range) increases as a function of L^2/λ where L is the aperture and λ the acoustic wavelength. In many practical cases, this minimum distance can be tens or hundreds of yards. Figure 3.2-2 shows how a near-field target results in a spherical wavefront and how this sphericity must be corrected by focussing, i.e. by adding the appropriate time delay.

The current C3D performs focussing by two extra curve sections located on the chip. This is sketched in Figure 3.2-3. By choosing appropriate frequencies f_c and f_d, near-field focussing can be performed for any given range R. In a pulsed system, signals coming in at later times represent returns from targets at increasing ranges. By changing clock frequencies f_c and f_d, the C3D can vary the focussing range with the increasing time. As $R \rightarrow \infty$, the wavefront becomes planar. Then f_c becomes equal to f_d and no focussing is performed.

This variable near-field focussing would be very difficult to achieve with LC delay line techniques. Thus the C3D has a unique performance capability for near-field high-resolution sonar beamforming.

Figure 3.2-4 shows a return from an off-axis near-field target as it impinges on the array. Succeeding steps show how the charge packets with the wavefront information are shifted in the array with time. Steps 1 through 5 show the beamsteering portion of the process. Step 6 shows some of the charge packets being shifted into the focussing section of the C3D. Focussing continues

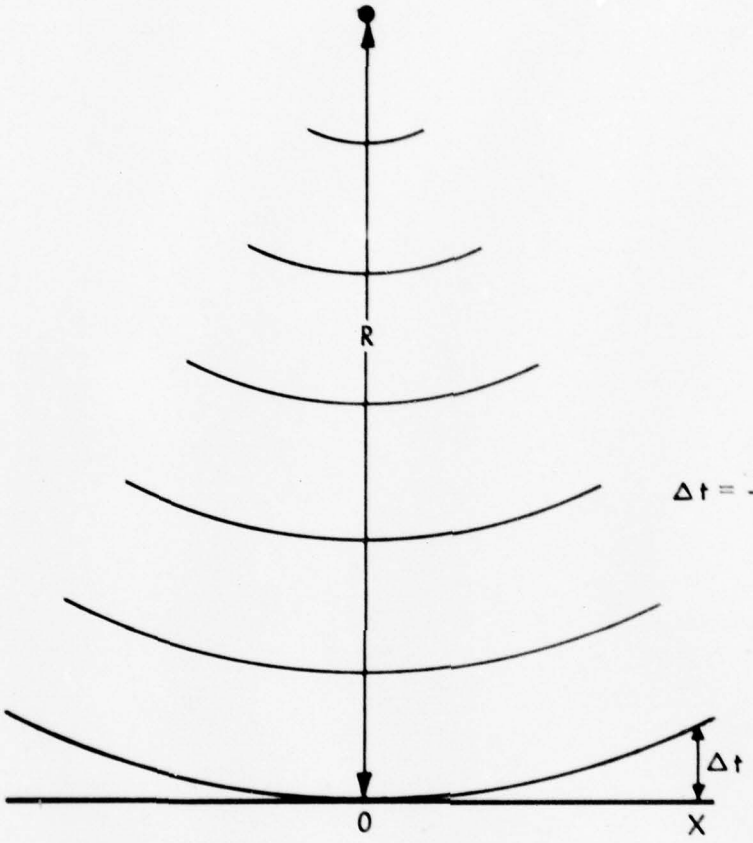


Figure 3.2-2. Spherical Correction for a Near-Field Target

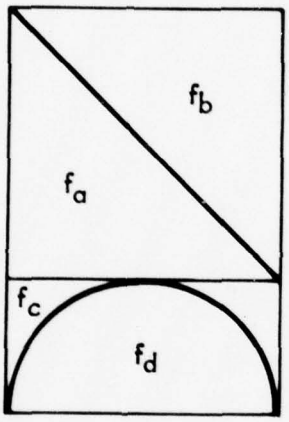


Figure 3.2-3. C3D Sketch with Beamforming and Focussing Sections

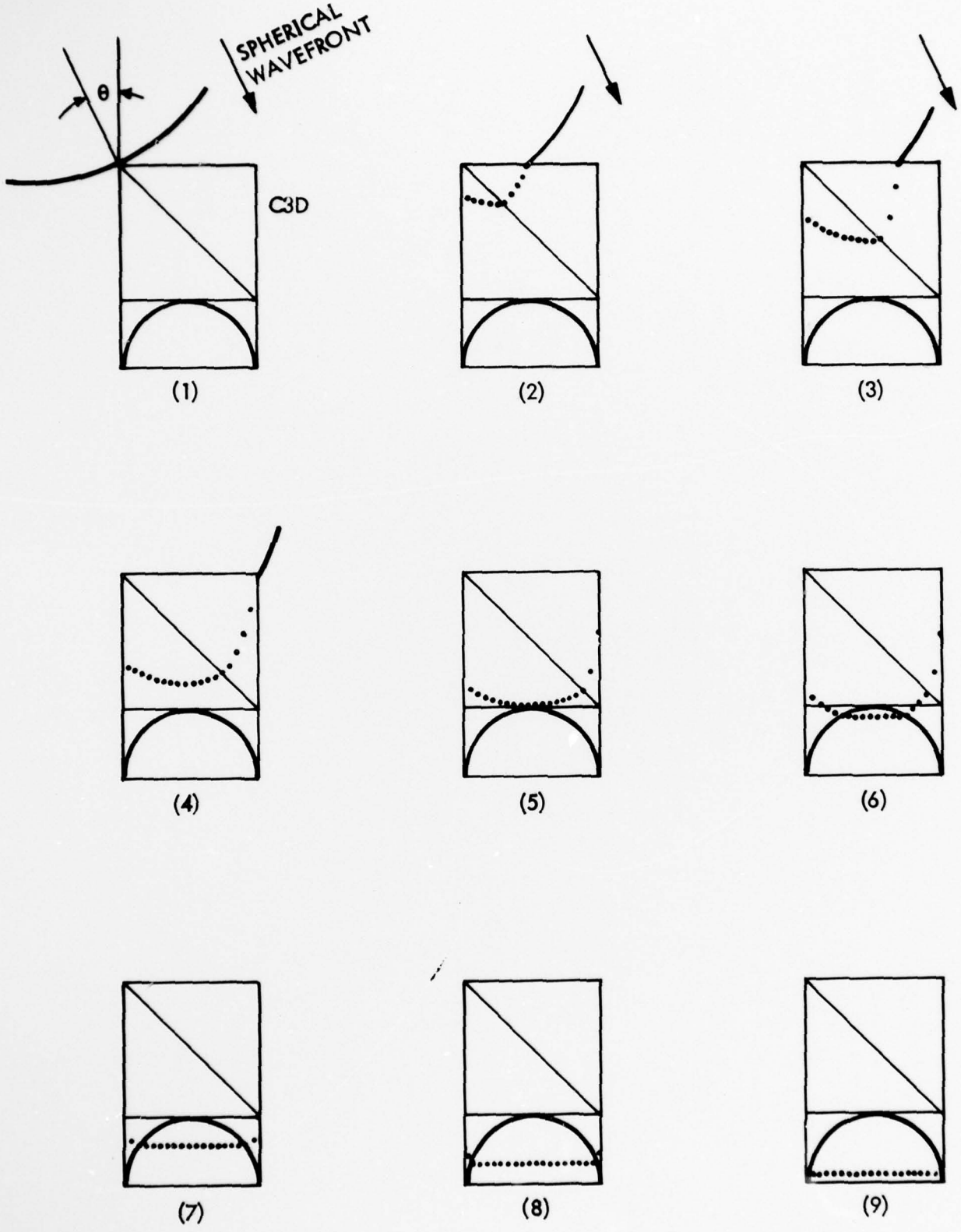


Figure 3.2-4. C3D Intermediate Stages of Beamsteering and Near-Field Focussing

in steps 7 and 8 until by step 9 all of the charge packets are in the same bit in each register. After step 9, the charge packets can be easily summed by removing the barriers between the parallal shift registers and dumping all the charges into the same gate. (Actually the current C3D begins summing the charge packets as soon as they reach "d" section clocked at f_d. This stage begins in step 6 of the figure.)

Another possible use of the focussing section of the C3D is to compensate for cylindrical arrays. Such arrays are considered useful in high resolution sonar because their resolution does not degrade for off-axis returns.

Thus the C3D represents a simple means of compensating for different times of arrival and then summing. This is the essence of beamforming. In addition, it can easily perform near-field focussing or cylindircal array correction.

Figure 3.2-5 is a microphotograph of a twenty-input C3D device.

3.3 Experimental Results.

Acoustic experiments at Stanford University at 1.5 MHz show that the device forms beams with theoretical sidelobes and a dynamic range of about 50 dB.

Experiments at Bendix at 180 KHz showed beamforming with -10 dB sidelobes instead of the theoretical -13 dB. The useable input signal level range is about 5 mV to 500 mV (peak-to-peak) indicating a dynamic range of at least 40 dB.

The device was tested at Bendix using a simulated input wavefront. The first tests were performed by applying the same signal to each of the twenty inputs on the device, simulating an on-axis acoustic return. The clock frequencies (all between 720 kHz and 3.0 MHz) were chosen to allow beamforming for a 180 kHz array of 3^o resolution and a $\pm 30^o$ field of view.

The clock frequencies were chosen in accordance with the following constraints. They must be multiples of 2/3 of the signal frequency. This is required because of nonlinearities inserted at the interface between the

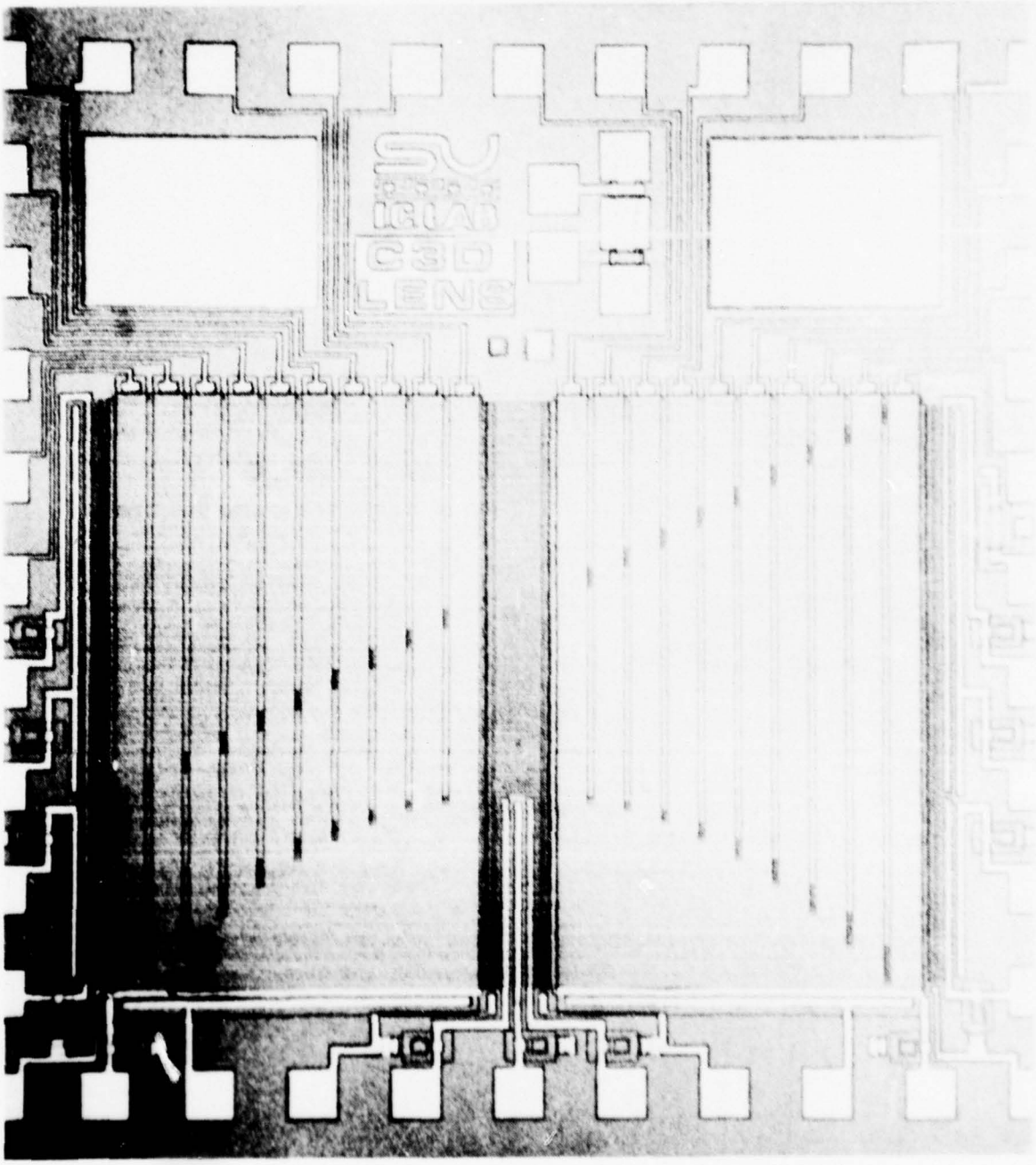


FIGURE 3.2-5 Microphotograph

various sections. Difference frequencies arise because the sample signal is being resampled at the boundary between the differently clocked sections. Spectral components will be found at the fundamental and higher order harmonics of the difference frequency between the clocks f_a and f_b. These difference frequency components arise because the transfer of charge across the f_a/f_b boundary is sensitive to the phase of f_a relative to f_b. This results in a non-uniform distribution of the originally uniform fat-zero charge. This appears as an additional output signal component.

Choosing clock frequencies that are multiples of 2/3 the input signal frequency prevents any sum or difference frequency components being formed at the same frequency as the original signal. As an example, the first tests at Stanford Unviersity were conducted at an acoustic signal frequency of 1.5 MHz so all the clocks were multiples of 1 MHz. Any possible sum or difference frequencies that could be generated by any combination of clock frequencies therefore were also multiples of 1 MHz. Thus, these frequency spikes did not interfere with the 1.5 MHz signal.

At Bendix we are applying an input signal at 180 kHz; accordingly, our clocks are all at frequencies that are multiples of 120 kHz.

The C3D chip has a beamforming section 47.5 bits in length. For elements #0 and #19 where all 47.5 bits are clocked at either f_a or f_b. The total delay time between signals entering and leaving the beamforming section is $47.5/f_a$ or $47.5/f_b$ respectively. A table was generated showing all the possible pairs of frequencies ranging between 720 kHz and 3.0 MHz and the end element delay time differences. These were compared to the theoretical delay ($\Delta T = L \sin \theta / v$) for each beam direction and used to choose appropriate clock pairs. (See Table 3.3-1.) In our case, L is equal to 15.9 cm, θ is the beam angle and v is the sound velocity (1500 m/sec). Note that many of the clock frequencies can be used for more than one beam. By simply reversing

TABLE 3.3-1

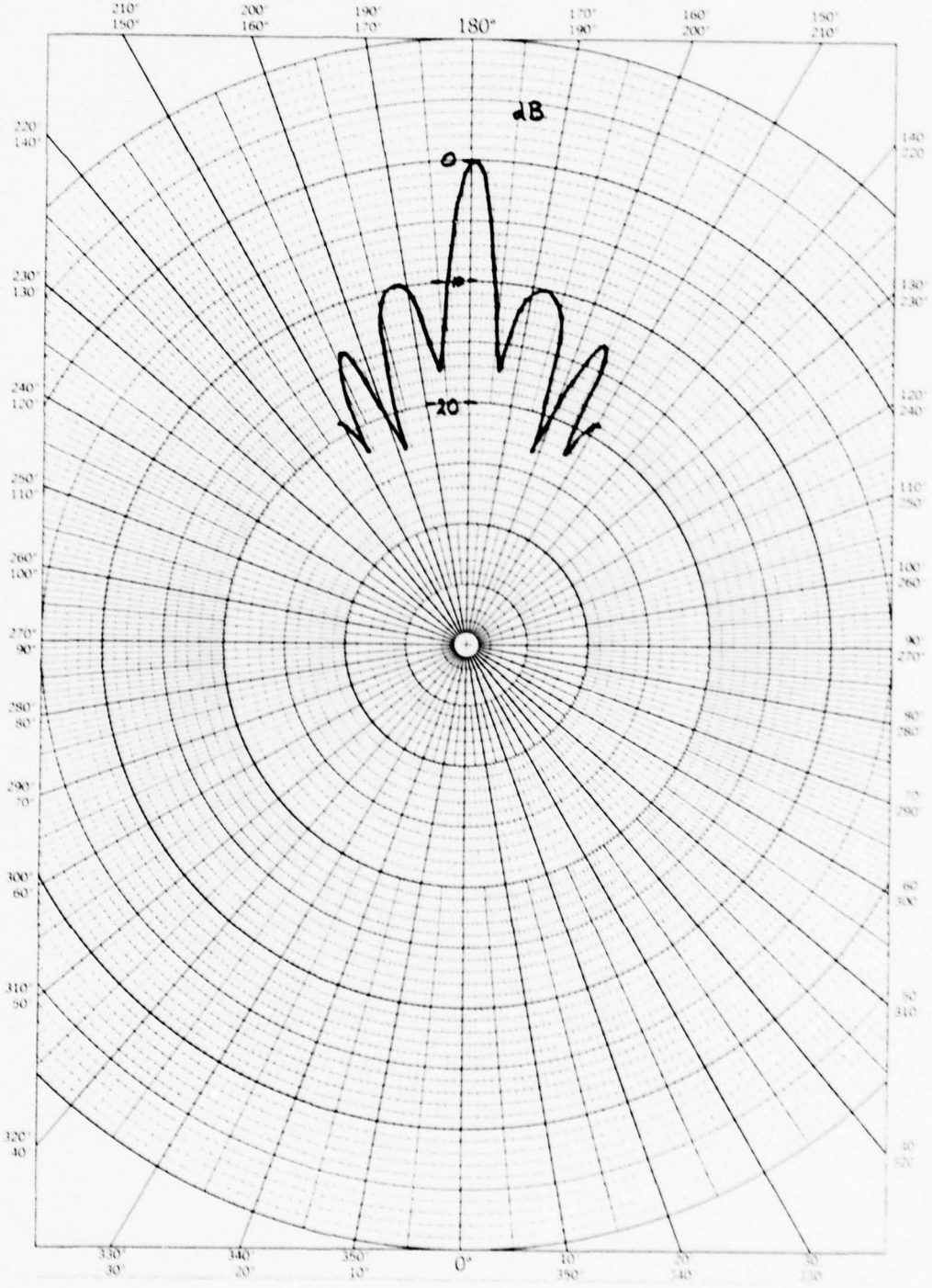
Theoretical Beam Angle	Theoretical Delay (μsec)	Clock 1 (MHz)	Delay 1 (μsec)	Clock 2 (MHz)	Delay 2 (μsec)	Actual Time (μsec)	Actual Beam Angle
0^o	0	--	--	--	--	--	--
3^o	5.5	2.28	20.8	3.00	15.8	5.0	2.8^o
6^o	11.0	1.80	26.4	3.00	15.8	10.6	5.8^o
9^o	16.5	1.44	33.0	2.76	17.2	15.8	8.6^o
12^o	21.9	.84	56.5	1.32	36.0	23.5	12.8^o*
15^o	27.3	.84	56.5	1.56	30.4	26.1	14.3^o
18^o	32.5	.96	49.5	2.52	18.8	30.7	16.9^o
21^o	37.7	.84	56.5	2.28	20.8	35.7	19.7^o
24^o	42.8	.84	56.5	3.00	15.8	40.7	22.6^o
27^o	47.8	.72	66.0	2.28	20.8	45.2	25.3^o
30^o	52.7	.72	66.0	3.00	15.8	50.2	28.4^o

* Although these frequencies are best at 12^o, to save on the number of crystal-controlled oscillators needed, .96 and 1.56 MHz were used, resulting in beam angle of 10.4^o.

the clock pairs at $\pm\theta$, a beam at $-\theta$ is generated. Also note at 0^o any frequency can be used and it is applied to both sections.

For these first experiments the two focussing sections were clocked at the same frequency, thus eliminating focussing since the input is a simulated planar wavefront.

Figure 3.3-1 shows the C3D response to the simulated on-axis planar wavefront. The input was held constant while the clocks were varied to 'scan' the field of view. The fact that the side lobes are only 10.0 dB down instead of the theoretical 13 dB is probably due to the fact that the gain of the device varies with the clock frequencies. Figure 3.3-2 shows the gain of the device versus clock frequency when all four sections of the device are clocked at the



Inputs all the same (simulating on-axis plane wave).
Steering section steered in indicated directions.
No compensation for different gains at different frequencies.

Figure 3.3-1 C3D BEAMFORMING

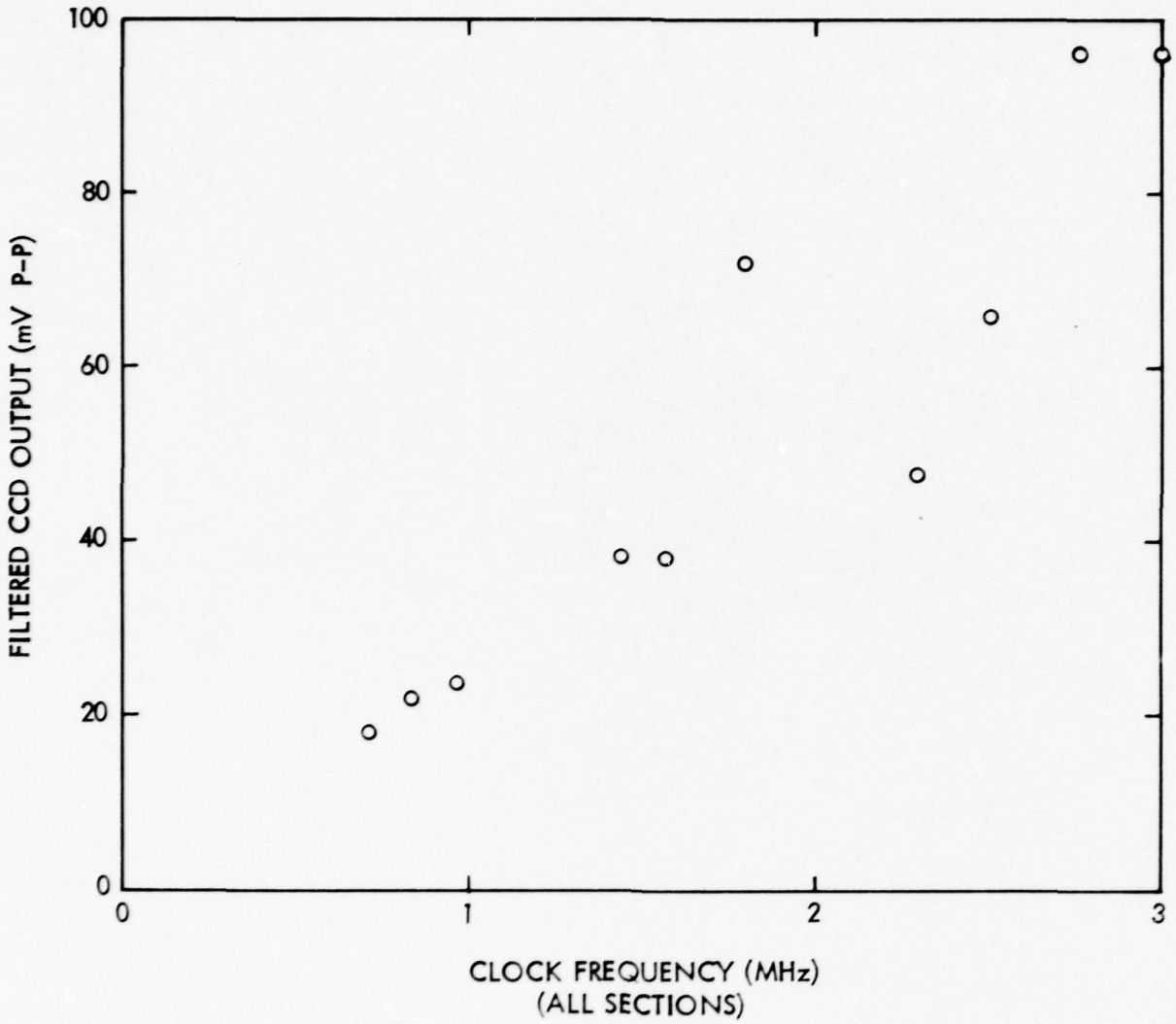


Figure 3.3-2. C3D Gain vs Clock Frequency

same rate. Figure 3.3-3 shows the gain versus clock frequency when both beamsteering sections are clocked at the same rate and the clocks on both focussing sections are held at 3.0 MHz. (Experiments at Stanford at clocking frequencies of ~20-30 MHz showed a much more constant gain characteristics.)

Another test of the C3D at 180 kHz was output linearity with respect to the input. Figure 3.3-4 shows the output versus input signal levels over a range of 5 to 500 mV. The experimental curve shows good linearity of the output with relation to the input. Note that in the 200 to 300 mV input level region there appears to be slight deviation from a straight line.

Effects of clock levels (which affect depth of potential wells) on device output were also studied. Figure 3.3-5 shows how the output varies with clock voltages, increasing as expected with the clock voltages and the MOS gate capacitance.

Measurements were made of the device dynamic range, but this turned out to be very difficult to perform experimentally and is easily subject to misinterpretation.

A spectrum analyzer was used so that signal output could be distinguished from clock frequencies and the measurement was based on the difference between the noise floor and the maximum signal level achieved in the region where the output signal was still linear with respect to the input level.

One of the dynamic range tests was conducted with all sections of the C3D being clocked at 3 MHz. This was performed with an HP 141T display, 8553B Spectrum Analyzer - RF section, and 8552B Spectrum Analyzer - IF section. Bandwidth on the spectrum analyzer was set at 10 kHz which would be a reasonable system bandwidth for a 180 kHz sonar.

The spectrum analyzer showed that there were many extraneous frequencies being introduced into the system due to clock drivers. Some measurements were made at 300 kHz because of a noise spike that occurred at 180 kHz. This

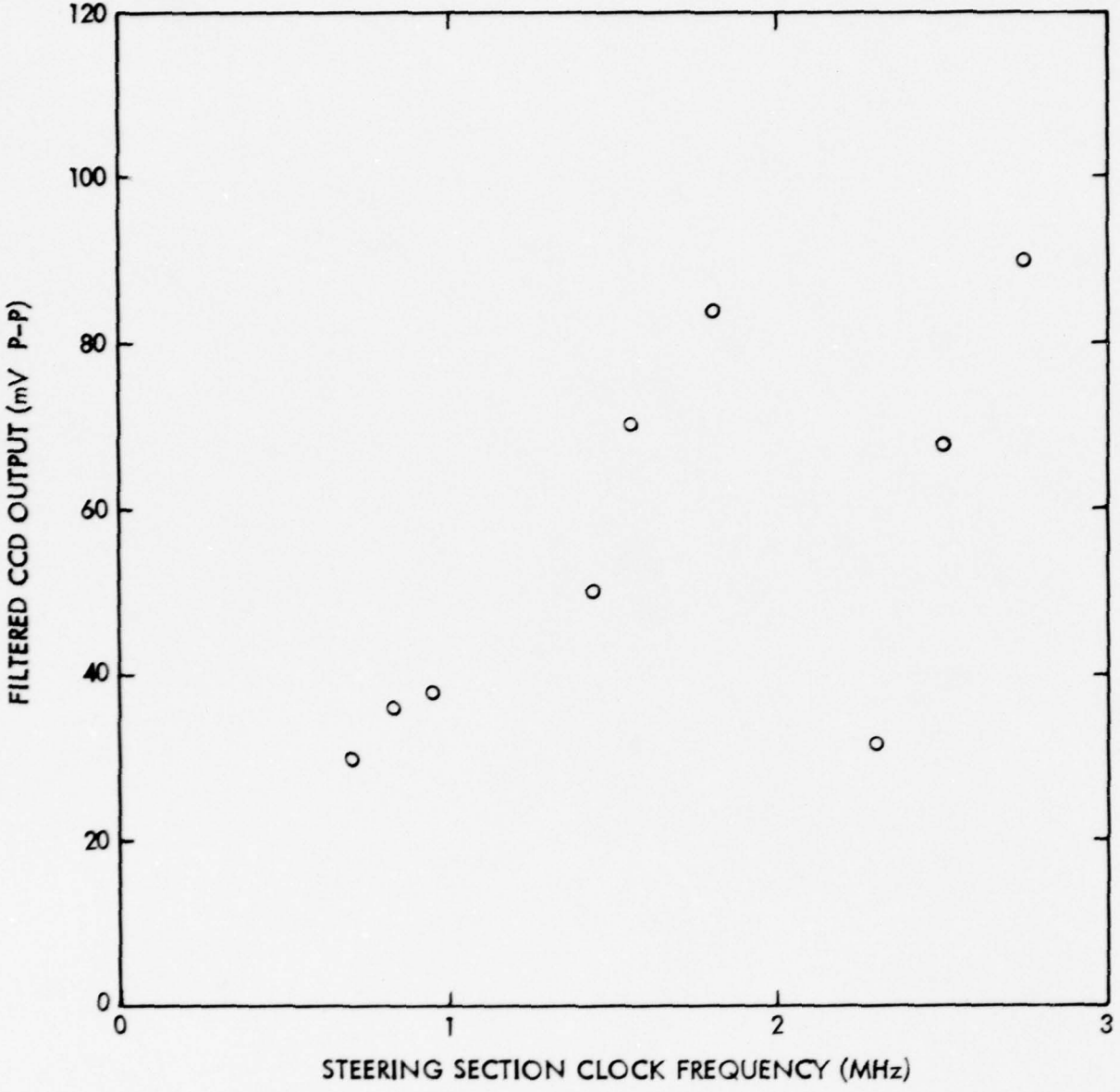


Figure 3.3-3. C3D Output vs Clock Frequency
(Focussing Section Constant)

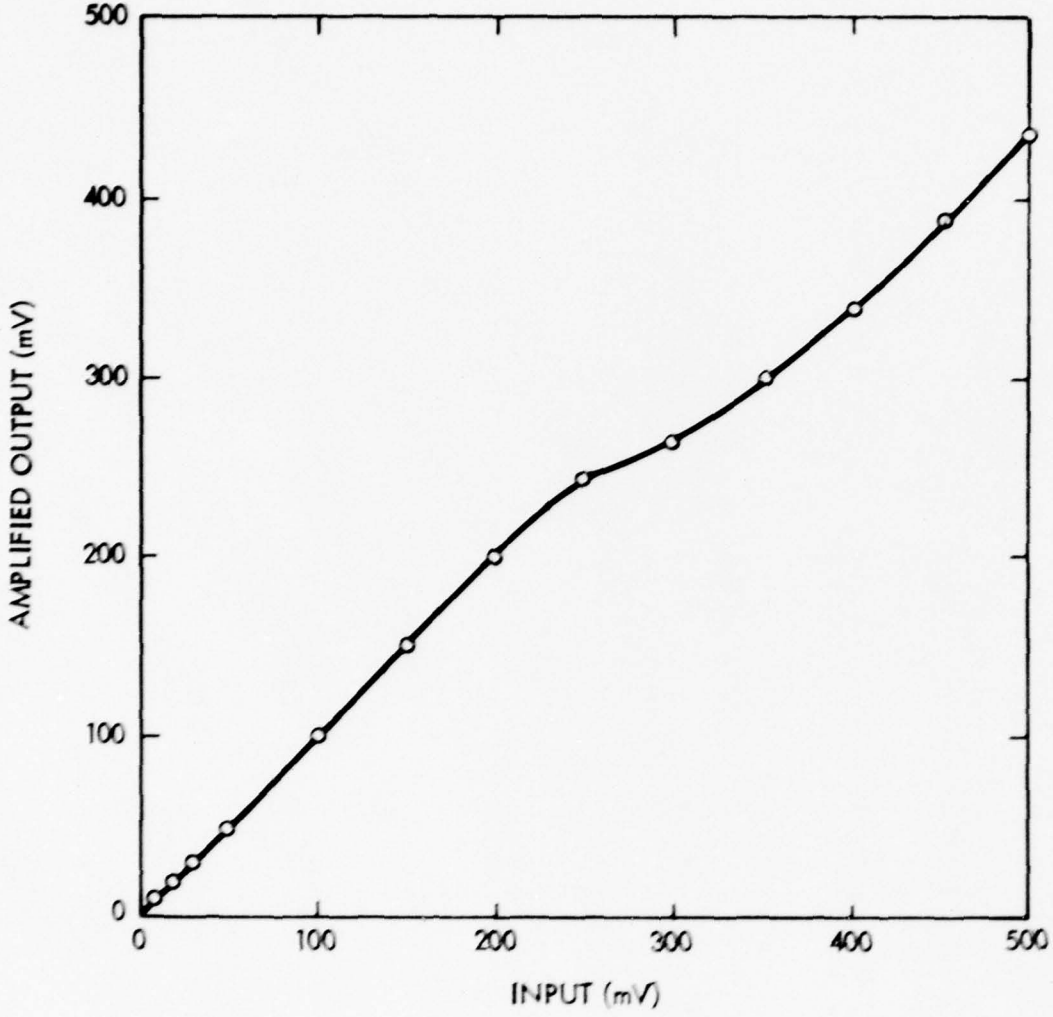


Figure 3.3-4. C3D Output Levels vs Input Levels

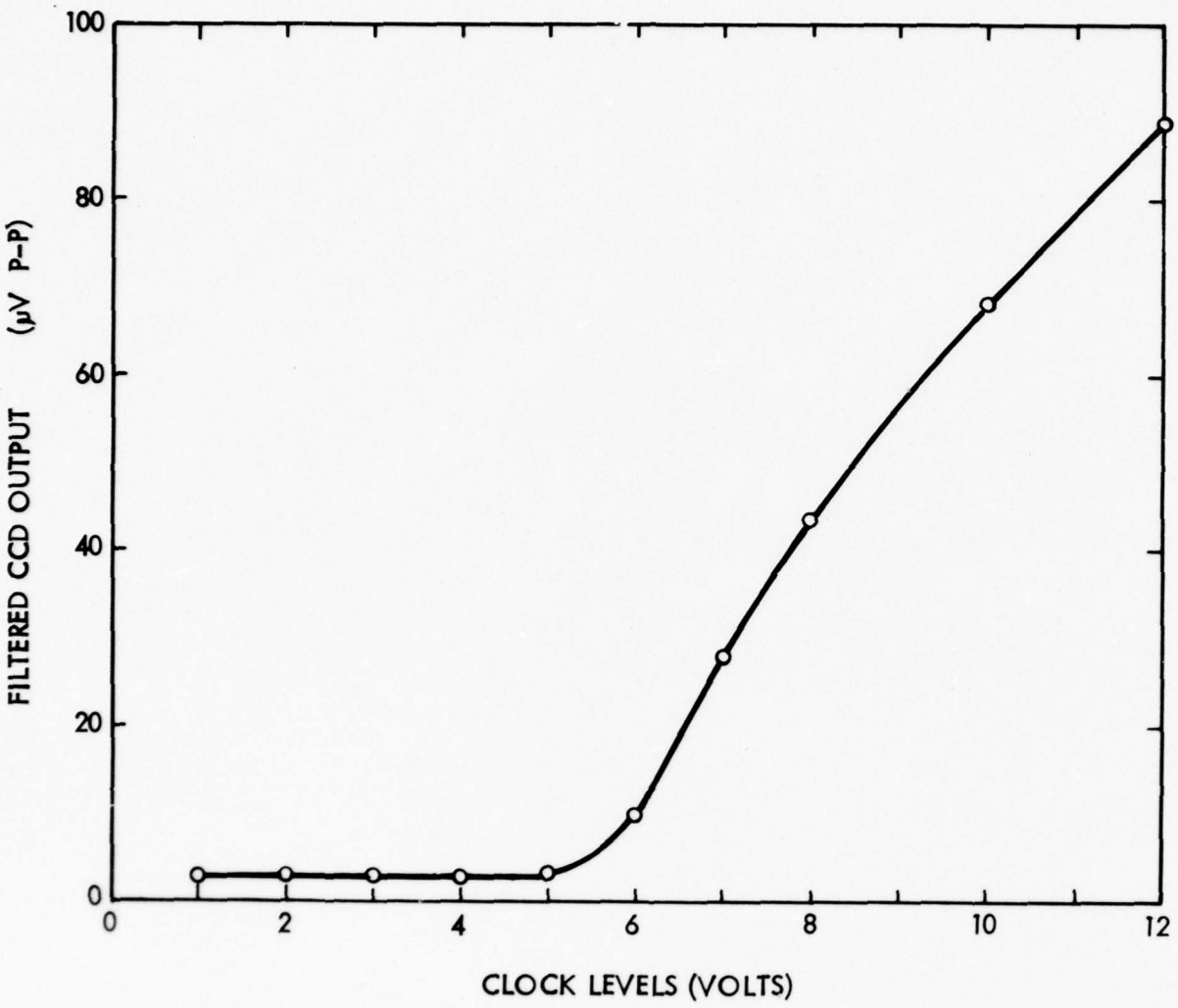


Figure 3.3-5. C3D Gain vs Clock Levels

experiment showed about 70 dB peak signal to peak noise ratios for a 10 kHz bandwidth with all clocks at 30 MHz. This fell off to about 60 dB for lower clock frequencies of 720 kHz.

These dynamic ranges are adequate for sonar beamforming when used in conjunction with either automatic gain control or time variable gain. However, further work is recommended to try to improve the dynamic range so that the C3D can be used alone.

At lower clocking frequencies, it was postulated that the decrease in dynamic range was caused by thermal relaxation effects (see section 2.3.2). An experiment was performed to measure the effect of cooling the CCDs (with thermoelectric devices). The cooling did appear to slightly improve the dynamic range of the devices, but the tests showed too much inconsistency to consider the results totally dependable. (Also, it should be noted that the high power consumption of the cooling devices, e.g. several watts required to cool a CCD chip by ~10°C to 20°C, may outweigh the power-saving advantages of CCDs in a low frequency beamforming system.) It is recommended that further cooling investigations be conducted using improved test equipment to rigorously characterize the device performance at low temperatures.

However, the cascade charge coupled device has already been shown to perform time-delay beamforming functions at typical high resolution sonar frequencies. If cooling does prove to increase the C3D dynamic range at lower frequencies (perhaps those typical of torpedoes), these devices may be extended to many kinds of sonar systems.

3.4 C3D Conclusions

This study has shown that a custom-designed CCD chip can now be applied to a time-delay sonar system under controlled conditions. Further work is recommended to improve fabrication techniques to increase the dynamic range of these devices. In addition, further work should be done in device measurement techniques, especially at low temperatures. With anticipated improvements in cascade charge coupled devices, it is likely that they will be applied to a wider range of multi-element time-delay sonar beamformers.

4.0 CHARGE COUPLED PROCESSOR.

The CCP was developed to perform the functions of a channel processor for a phase-delay 'holographic' beamforming system. These functions are: Amplification, mixing, integration, and filtering. A channel processor converts the AC signal from an array hydrophone to a pair of DC signals corresponding to the complex phase and amplitude. Processing of the array data can then be performed with digital hardware or software.

This section discusses phase-delay beamforming, the CCP channel processor operation and its experimental results.

4.1 Phase-Delay Beamforming.

A phase-delay beamformer performs the same functions of delay and summation as a time-delay beamformer described in section 3.1. However, instead of applying a time delay by analog circuits, an equivalent phase delay is inserted by digital circuitry.

Figure 3.1-1 showed how an off-axis wavefront arrived at element #0 a time $\Delta t_n(\theta)$ before reaching element #n. This time was shown to be:

$$\Delta t_n(\theta) = \frac{nd \sin \theta}{v} \qquad (4.1\text{-}1)$$

This time delay shift can be converted to a phase shift by multiplication by $2\pi f$. Thus:

$$\Delta \phi_n(\theta) = 2\pi f \ \Delta t_n(\theta) \qquad (4.1\text{-}2)$$

$$= \frac{2\pi f \, nd \sin \theta}{v}$$

$$= \frac{2\pi \, nd \sin \theta}{\lambda}$$

Note how the frequency (and wavelength) are terms in this equation and therefore must be known. This generally limits phase-delay beamforming to

active narrow-band systems. However, there are advantages to this approach as will be discussed later.

Assuming that $A_n \exp(\Psi_n)$ represents the complex signal on element n and Ψ_n is the phase term, a phase shift of $-\Delta\emptyset_n(\theta)$ will be applied to compensate for the delay. These terms are then summed to give the beam in direction θ.

$$S(\theta) = \sum_{n=0}^{N-1} A_n e^{j(\Psi_n - \Delta\emptyset_n(\theta))} \qquad (4.1\text{-}3)$$

$$= \sum_{n=0}^{N-1} A_n \exp\left(j\Psi_n - j\frac{2\pi}{\lambda} nd \sin\theta\right)$$

$$= \sum_{n=0}^{N-1} A_n \exp(j\Psi_n) \exp\left(-j\frac{2\pi}{\lambda} nd \sin\theta\right)$$

Thus the beamforming can be seen to be a multiplication of the signals $A_n \exp(j\Psi_n)$ with $\exp\left(-j\frac{2\pi}{\lambda} nd \sin\theta\right)$, then a summation. If the signals $A_n \exp(j\psi_n)$ are known, this multiplication and summation can be performed digitally. Such functions as near-field focussing and gain correction can also be performed by digital multiplication by the appropriate amplitude and phase factors. In addition, by doing the phase-delay computations in digital software, there is the flexibility to apply different array shadings, superresolution calculations, etc.

The function of the Charge Coupled Processor is to convert the AC signal on the n th element to a DC term proportional to $A_n e^{j\Psi n}$ and output it to the digital processor. The processes required to do this are mixing and integration.

Mixing consists of multiplying the incoming AC signal by a reference signal of the same frequency. The signal at time t is:

$$A_n \sin(\omega t + \Psi_n)$$

Multiplying by the sine of reference signal gives:

$$A_n \sin(\omega t + \Psi_n) \sin \omega_r t$$

Applying the trigonometric identity:

$$(\sin x)(\sin y) = 1/2 \quad [\cos(x-y) - \cos(x+y)] \qquad (4.1\text{-}4)$$

we get: $A_n \sin(\omega t + \Psi_n) \sin(\omega_r t)$ (4.1-5)

$$= \frac{A_n}{2} \left[\cos(\omega t + \Psi_n - \omega_r t) - \cos(\omega t + \Psi_n + \omega_r t)\right]$$

and since $\omega_r = \omega$:

$$= \frac{A_n}{2} \left[\cos \Psi_n - \cos(2\omega t + \Psi_n)\right]$$

Note that we have an expression containing frequencies representing the sum and difference between the signal and reference frequencies. The first term is a zero-frequency term (or constant) while the second has a frequency of 2ω. By integrating over time, the second high-frequency term goes to zero while the first term increases proportionally to the integration interval. This term becomes:

$$kA_n \cos \Psi_n \qquad \text{(where k is a constant)}$$

Note how this contains both the amplitude A_n and phase term Ψ_n.

By multiplying $A_n \sin(wt + \Psi_n)$ by the cosine of the reference signal we get:

$$A_n \sin(\omega t + \Psi_n) \cos(\omega_r t) \qquad (4.1\text{-}6)$$

$$= \frac{A_n}{2} \left[\sin(\omega t + \Psi_n - \omega_r t) + \sin(\omega t + \Psi_n + \omega_r t)\right]$$

$$= \frac{A_n}{2} \left[\sin \Psi_n + \sin(2\omega t + \Psi_n)\right]$$

Again by integration over time, the second term goes to zero leaving a DC term:

$$kA_n \sin \Psi_n$$

Both terms $kA_n \sin \Psi_n$ and $kA_n \cos \Psi_n$ are needed to determine A_n and Ψ_n.

Thus a channel processor must mix and integrate to get the complex signal values for the solution of equation (4.1-3). Multiplexing involves the ordered outputting of these quantities to the digital processor that solves the equation.

Channel processors which mix and integrate also filter because the reference signal frequency must equal the signal frequency for maximum output (as can be seen in equations 4.1-5 and 4.1-6).

The mixing operation can be replaced by using quadrature sampling. By sampling at time t and also $t + \frac{T}{4}$ (where T is equal to 1/f, i.e. the period), we get a term containing $A_n \cos (\Psi_n + \phi_r)$, $\left[\phi_r \text{ is an arbitrary phase}\right]$ and a term, $A_n \cos (\Psi_n + \phi_r + \frac{\pi}{2})$, which equals $A_n \sin (\Psi_n + \phi_r)$.

By repeating the sampling over a number of cycles and summing, an integration is performed. This also serves to improve the signal-to-noise ratio.

The Charge Coupled Processor mixes by this sampling process. An operational description of the CCP will be given next.

4.2 CCP Operation Description.

The CCP uses three important characteristics of charge coupled devices.

1. CCD's can switch or gate a charge which is proportional to an injection voltage at a specific point in time. This sampling of the gated input signal results in a stored charge proportional to the amplitude and sine or cosine of the phase of an input signal. Two CCP channels are needed to get both $A_n \cos \Psi_n$ and $A_n \sin \Psi_n$ so that $A_n e^{j\Psi n}$ can be used to solve equation 4.1-3.
2. CCD's can sum or integrate the charges by shifting the injected charges into a potential well that is held stationary during the integration interval.
3. CCD's can gate the charge summation to an output register providing a simultaneous sensing and resetting of the channel processor integrator.

In addition to the above three processor functions, the CCD forms an analog shift register which multiplexes the gated charges stored in the integrators to a single out connection.

Figure 4.2-1 shows a partial schematic of the Charge-Coupled Processor. The device fabricated during Phase 1 has four channels and can form both sine and cosine terms for two inputs (or either sine-only or cosine-only terms for four inputs).

For simplicity, the figure shows just one of the inputs.

The diode connected to pad 10 acts as the source for the charge-coupled device. It is called the launch diode. In a sonar application, a hydrophone/ preamplifier output voltage would be the input to pad 10. The launch diode injects charges into the channel when a bucket (or potential well) is formed under the bias gate connected to pad 11. The next two gates (12 and 13) are the launch gates. (During normal operation they are tied together. However, the device was designed to allow them to operate independently.) The launch gates are used as the mixing gates and are connected to either the sine or cosine reference signals. The sum of the charges from gates 12 and 13 is stored under the first clock gate connected to pad 21, the phase 1 clock input. The well is held stationary during the integration time.

After the integration is complete, the well beneath the launch gate is removed, leaving the sum charge under pad 21, the first clock gate. At the beginning of the shift phase, the Phase 1 and Phase 2 (Ø1 and Ø2) clocks are turned on and the charge contained under the first gate of the Ø1 clock shifted down the shift register to the output diode connected to pad 15. Pad 14 is the output bias gate which controls the charge threshold transferred into the output diode. After the charge contained at the output diode is sensed by the output amplifier connected to pads 18 and 19, the reset gate connected to pad 16 is

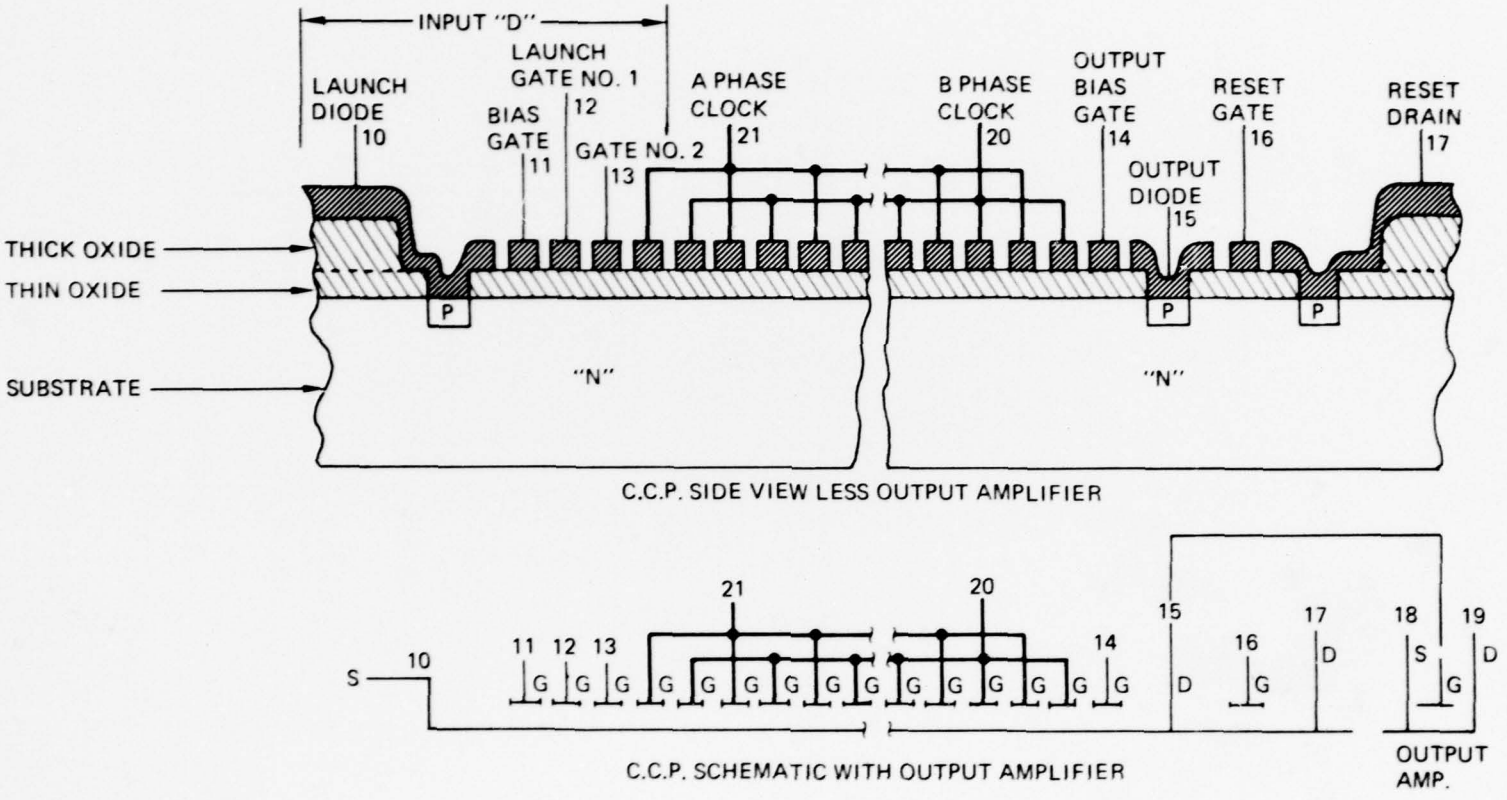


Figure 4.2-1 Charge Counled Processor (CCP)

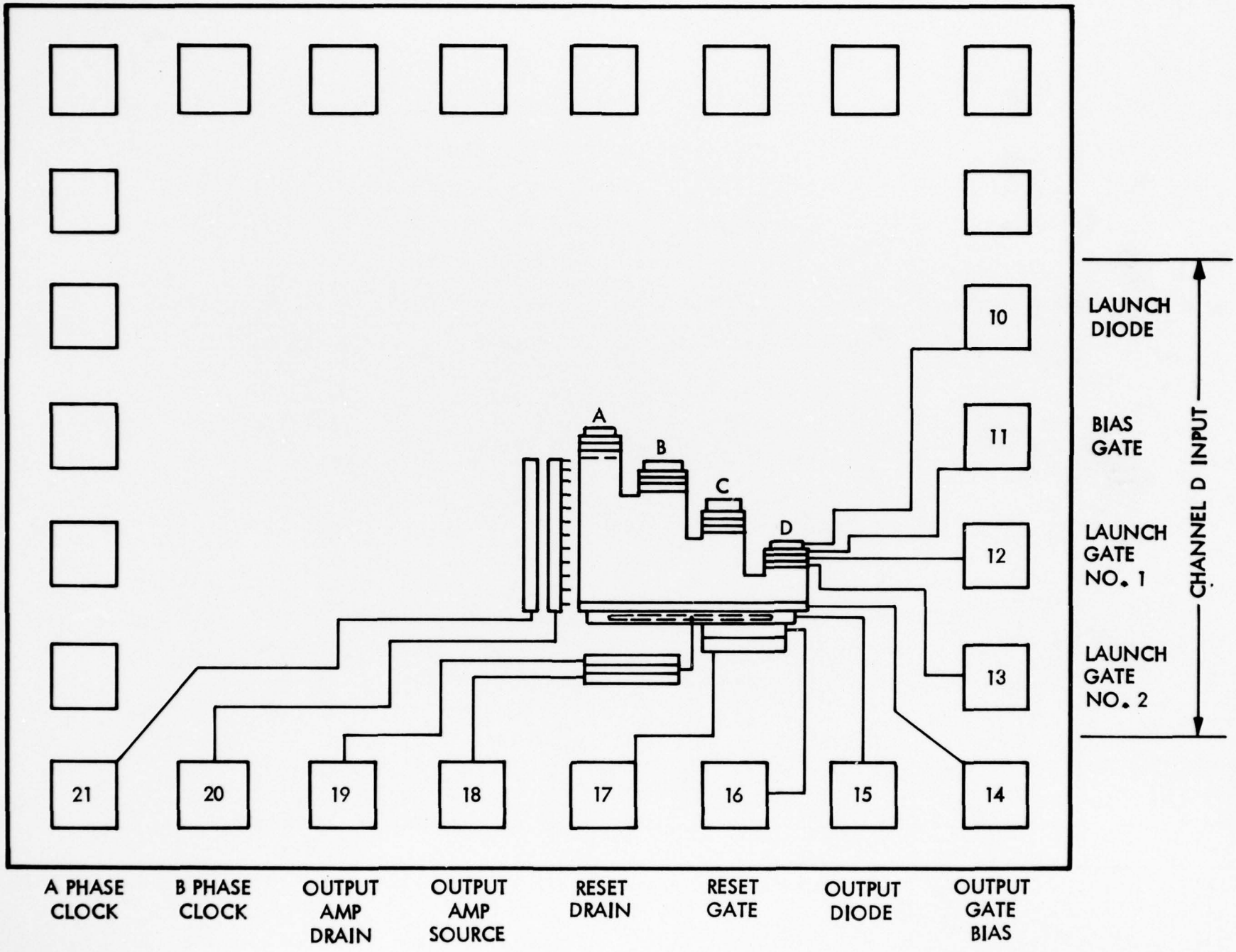


Figure 4.2-2. Partial Layout of CCP

turned on and discharges the stored charge at the output diode into the reset drain diode connect to pad 17. For this "D" channel, there are four Ø1 clock gates and four Ø2 clock gates (or four bits total) between the launch gate and the output bias gate.

Figure 4.2-2 shows partial physical layout of the CCP test device.

The signals start at the top of the charge coupled processor and shift their way down to the output at the bottom. The clock gates connected to pads 20 and 21 cross horizontally over the 'stair step' shift register portion of the charge coupled processor. As described previously, four gate pairs cross over the "D" section (for one of the four inputs) of the charge coupled shift register. Each input is separated by four additional gate pairs or bits, therefore, the "C" input contains eight bits in its shift path while the "B" and "A" inputs contain twelve and sixteen respectively. When the Ø1 and Ø2 clocks are turned on during the shifting sequence, the charges stored under the adjacent Ø1 clock for each input are shifted down to the output diode. As the "A" input requires sixteen clock sequences to reach the output diode and "D" requires only four, the "D" output will arrive at the output diode twelve clock cycles before the "A" output. The result is a serial train of stored charges starting with "D" input and ending with the "A" input, each separated in time by four clock cycles. The purpose of these extra clock steps between the input and output is to provide better channel-to-channel isolation. Thus, the device converts the parallel inputs to serial outputs, which provide multiplexing capabilities.

The purpose of the four bit separation is to provide adequate charge isolation between individual inputs. This is necessary in the CCP because there is a certain amount of charge transfer inefficiency due to trapped charges or surface states. After each clock shift, a few of the charges are left behind

which would be added to the charges from the next input if not separated. Also, this separation is important in the case of saturation, i.e., when the charges fill the potential well and there is overflow to adjacent wells.

Even though the addition of four bits between each input requires an increased clock frequency (to maintain the same through-put time), the isolation it gives is important and was verified during device evaluation.

Figure 4.2-3 is a microphotograph of the Charge Coupled Processor. The left-hand portion is an unrelated experimental preamplifier which is "piggybacking" on the CCP chip.

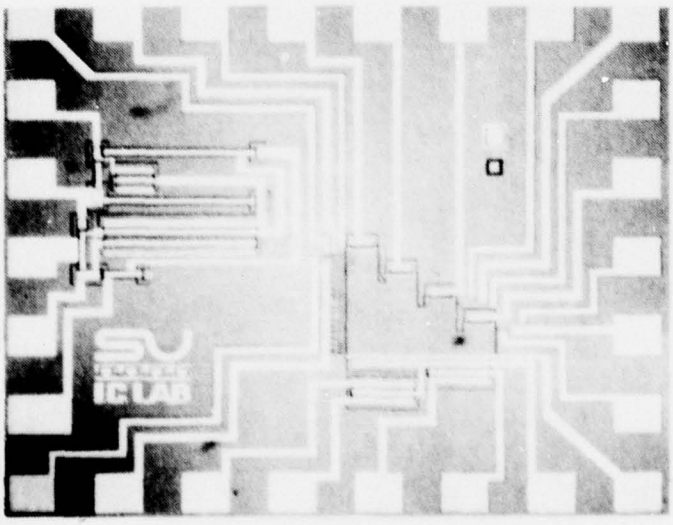


Figure 4.2-3. Microphotograph of CCP

4.3 CCP Experimental Results

Experimental results from the Charge Coupled Processor tests showed that the unit does perform the mixing, integration, and amplification functions. Filtering is inherent in the mixing and integration functions as shown in section 4.1. Measurements of the device operating characteristics when operating as a channel processor showed the existence of subtle transconductance characteristics which had not been known for CCDs before. Some of the tests on the device at 200 kHz are described next.

The first tests were undertaken to determine which of the twenty packaged devices exhibited best channel uniformity. The best chip, number B2, was chosen for the initial tests. Subsequent tests were also performed with several other chips and the results were relatively consistent.

The oscilloscope tracing in figure 4.3-1 represents the output of the four-channel device clocked at 200 kHz. During the first 40% of the sweep, the mixing and integration period, the output of the CCP is not meaningful. After the integration period the output gate is reset be external logic, and the next three pulses represent the miscellaneous charges from the channel separation gates described earlier. The next high pulse is the Channel D ouput. In this experimental setup, the clock and signal frequencies are not exactly the same, and the device output varies from sweep to sweep of the oscilloscope. Thus the peak-to-peak level in this picture can be compared to the input signal peak-to-peak level and used as a measure of the device gain. (The bias level of the output is the result of the injected bias current which will be discussed later.)

The succeeding sets of three low level pulses and one high level pulse each represent the charges from three separating gates and one processing channel. These channels which follow the "D" channel output are "C", "B", and "A" respectively.

After channel A is read out, the shifting sequence stops and there is no need to reset the output gate until the completion of the succeeding integration period when new outputs are available from channel D. At that time, the shifting sequence begins again and the output gate is reset after every output. Thus, the "pulses" which appear following the channel A output pulse (and during the integration period) are just succeeding readouts of the same signal level.

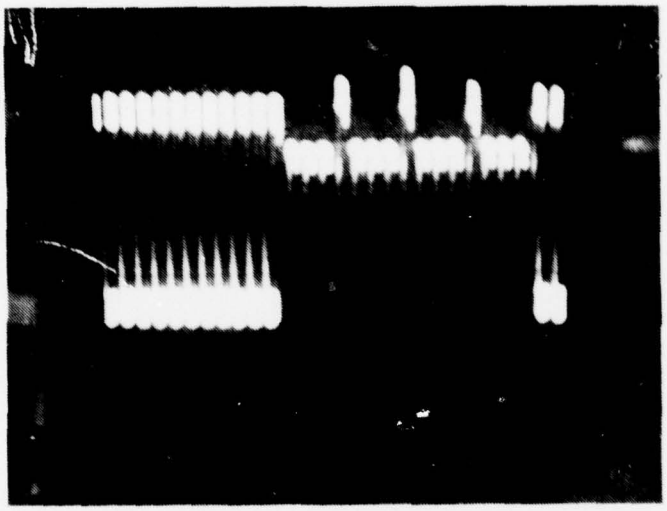


FIGURE 4.3-1 Output of Charge Coupled Processor

Figure 4.3-2 shows the input circuit for injecting the signal into the CCP. The variable input resistor gives control over the amount of bias current injected. This is also known as the 'fat zero.' Normally, a 'fat zero' is used to prevent the charges in a bucket from going to zero and operating in a manner such that charges are trapped by surface states. (See Section 2.3-1.) By adding a small bias current, the charge in the bucket is never zero and the signal to noise ratio is higher.

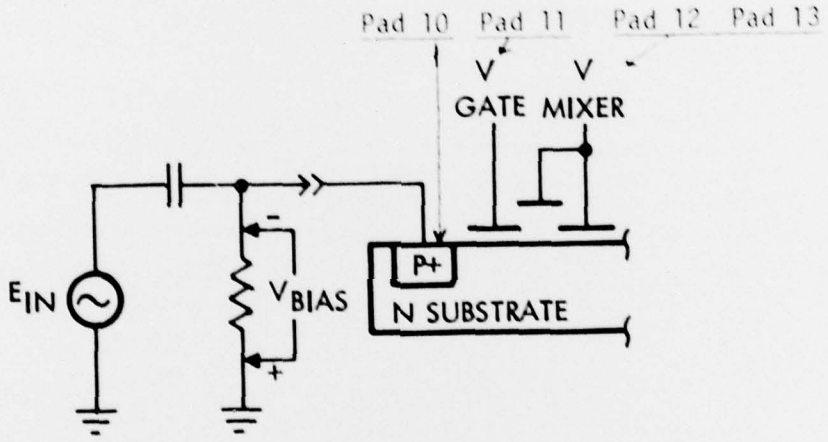


Figure 4.3-2. CCP Input Circuit

In the Charge Coupled Processor, the 'fat zero' is introduced because an AC signal is being sampled. Only positive charges are stored in the wells; hence the presence or absence of carriers represents signal information. Thus, a bias level corresponding to a zero signal level must be established which keeps the negative swings of the AC signal above the zero charge level in the wells.

To prevent the charge 'bucket' from overflowing when a number of samples are collected, the injection current per sample has to be lowered. In the case of the Charge Coupled Processor, this brings the current levels down into the subthreshold region of the transconductance curve where the output becomes linear with injected current. Although this linear effect has been observed for standard MOS devices, it is believed that this is the first time it has been measured in CCD device.

This effect results in a leveling off of the gain as the number of samples is increased.

To see how the linearity of the transconductance curve at low current levels affects the gain, consider the standard equation for transconductance in a MOS device: $g_m = K_1 \sqrt{I_s}$ (4.3-1)

where K_1 is a constant and I_s is the injected current level per sample. When one sample is taken, I, the total current, is equal to I_s. The total injection current is adjusted by the bias voltage to one-half the saturation current ($I = \frac{1}{2} I_{max}$), thereby operating the device in the center of its linear range.

To prevent saturation when N samples are collected, the gate bias voltage is reduced so that the injection current for each of the N samples I_s is the total injection current I divided by N.

$$I_s = I/N \qquad (4.3\text{-}2)$$

Substituting this into equation 4.3-1:

$$g_m = K_1 \sqrt{\frac{I}{N}} \qquad (4.3\text{-}3)$$

The device gain for N samples (i.e. the sum of the individual sample gains) is simply N times the average sample gain S, because each sample is the same.

The total gain is equal to the device gain times the transconductance:

$$G = g_m \times \text{device gain} \qquad (4.3\text{-}4)$$

$$= K_1 \cdot \sqrt{\frac{I}{N}} \cdot N \cdot S$$

Let $K_2 = K_1 \cdot I \cdot S$, then

$$G = K_2 \frac{N}{\sqrt{N}} \qquad (4.3\text{-}5)$$

$$= K_2 \bullet \sqrt{N}$$

Thus the total gain was expected to be proportional to the square root of the number of samples.

However, when many samples are integrated by the device, the resulting low level input current per sample (so that <u>total</u> current levels do not cause saturation) causes the device to operate in the <u>linear</u> region of the transconductance curve. This is where the transconductance is directly proportional to the input current per sample; thus:

$$g_m = K_1 I_s$$

As before, for N samples, $I_s = I/N$. Thus $g_m = K_1 \cdot I/N$. The total gain then becomes:

$$G = \text{device gain x transconductance} \qquad (4.3\text{-}6)$$

$$G = (N \cdot S) \cdot K_1 \cdot \frac{I}{N}$$

Again we let $K_2 = K_1 \cdot I \cdot S$, therefore:

$$G = K_2$$

In this case, the total gain is constant and increased integration times cannot improve output levels.

Figure 4.3-3 is a curve which shows the total gain as a function of the number of samples for the D input of device #B3. In this case, the experimental limit on the gain was 3.0.

For other devices, and other channels on the same device, the gain leveled off at different values between ~0.3 and ~3.0. The transition between the linear and square root portions of the transconductance curve varies from channel to channel with even slight physical variations on the gates. To get the required uniformity is beyond the present state of the art even for small chips. The fabrication of larger chips for multi-element arrays is not feasible with present technology.

The various channels also do not have as much individual gain adjustment. For example, the curve in Figure 4.3-3, for #B3, shows the gain variation on that device can only run between 0.7 and 3.0; thus it is not always possible to adjust the gains of different devices to the same levels.

It should be noted that these limitations on the device are not the result of noise but of the fact that the CCP is operated near the linear region of the transconductance curve.

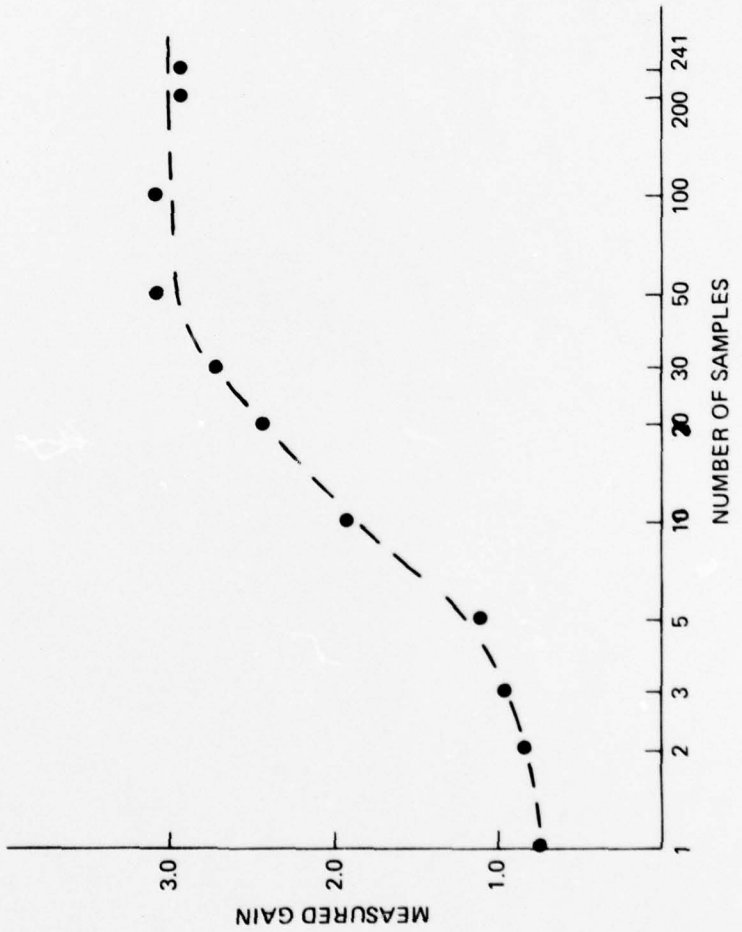


Figure 4.3-3 Measured Gain of CCP

We have shown how custom CCDs can be used to combine mixing, integration, and filtering functions on a single compact chip. With advances in fabrication state-of-the-art, these techniques should lead to a multi-channel CCP for phase-delay beamforming.

5.0 SUMMARY

Two types of CCDs for multi-element sonar beamforming have been fabricated and tested. The Charge Coupled Processor does mixing, integration, filtering and multiplexing on a single chip for a phase-delay beamforming system. Tests of a four-input device show successful performance of these functions. The Cascade Charge Coupled Device performs time delay and summation for 20-element sonar arrays.

This study has shown that custom CCDs can be applied to special sonar systems with current device state-of-the-art. It is recommended that further work be performed to improve dynamic range, fabrication processes, and device measuring techniques. With these improvements, it is expected that CCDs will play an important role in a wider range of sonar applications.

6.0 REFERENCE

"Charge Coupled Devices for Holographic and Beamsteering Sonar Systems," R. D. Mele, J. D. Shott, B. T. Lee and L. C. Granger, publ. in Acoustical Holography, Vol. 7, ed. by L. W. Kessler, 1977, Plenum Press.